

NI Signal Generators Help

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This help file contains information about the following topics:

- Fundamentals of waveforms and video signals
- <u>Device-specific</u> content for all NI signal generators
- <u>Getting started</u> steps for creating an application with NI-FGEN and your ADE
- <u>Programming references</u> for both <u>NI-FGEN</u> and the NI Composite Video Generator
- Interactive generation of <u>waveforms</u> and <u>video signals</u>

To download the latest versions of NI source documentation and examples, visit <u>ni.com/instruments</u>. For more information about this help file, refer to the following topics:

Using Help

Related Documentation

<u>Glossary</u>

Important Information

Technical Support and Professional Services

To comment on National Instruments documentation, refer to the <u>National</u> <u>Instruments Web site</u>.

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Related Documentation

Most signal generator manuals also are available as PDFs. You must have Adobe Reader with Search and Accessibility 5.0.5 or later installed to view the PDFs. Refer to the <u>Adobe Systems Incorporated Web site</u> at www.adobe.com to download Adobe Reader.Refer to the <u>National</u> <u>Instruments Product Manuals Library</u> at ni.com/manuals for updated documentation resources.

The following documents contain information that you may find helpful as you use your NI signal generator. The following links open PDF files.

- NI-FGEN Instrument Driver Readme File
- NI Signal Generators Getting Started Guide
- NI 5431 Video Generator Instrument Driver Quick Reference Guide
- <u>NI 5401 Specifications</u>
- <u>NI 5402/5406 Specifications</u>
- <u>NI 5402/5406 Calibration Procedure</u>
- <u>NI 5404 Specifications</u>
- <u>NI 5404 Calibration Procedure</u>
- <u>NI 5411/5431 Specifications</u>
- <u>NI 5412 Specifications</u>
- <u>NI 5412 Calibration Procedure</u>
- <u>NI 5421/5441 Calibration Procedure</u>
- NI 5421 Specifications
- <u>NI 5422 Calibration Procedure</u>
- <u>NI 5422 Specifications</u>
- <u>NI 5441 Specifications</u>
- <u>NI 5442 Specifications</u>
- <u>NI 54XX Calibration Procedure</u> (contains calibration procedures for the NI 5401/5411/5431)

Visit <u>ni.com/manuals</u> for the most current revisions of documentation and for newly released documentation.

Using Help

<u>Conventions</u> <u>Navigating Help</u> <u>Searching Help</u> <u>Printing Help File Topics</u>

Conventions

This help file uses the following formatting and typographical conventions:

- < > Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, AO <0..3>.
- [] Square brackets enclose optional items—for example, [response].
- The » symbol leads you through nested menu items and dialog box options to a final action. The sequence File»Page Setup»Options directs you to pull down the File menu, select the Page Setup item, and select Options from the last dialog box.
- The symbol indicates that the following text applies only to a specific product, a specific operating system, or a specific software version.
- This icon denotes a note, which alerts you to important information.
 - This icon denotes a tip, which alerts you to advisory information.
- This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.
- **bold** Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options.
- dark red Text in this color denotes a caution.
- green Underlined text in this color denotes a link to a help topic, help file, or Web address.
- *italic* Italic text denotes variables, emphasis, cross–references, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

monospace Text in this font denotes text or characters that you should

enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.

monospace Bold text in this font denotes the messages and responses
bold that the computer automatically prints to the screen. This font also emphasizes lines of code that are different from the other examples.

monospace Italic text in this font denotes text that is a placeholder for a *italic* word or value that you must supply.

Navigating Help (Windows Only)

To navigate this help file, use the **Contents**, **Index**, and **Search** tabs to the left of this window or use the following toolbar buttons located above the tabs:

- Hide—Hides the navigation pane from view.
- Locate—Locates the currently displayed topic in the Contents tab, allowing you to view related topics.
- **Back**—Displays the previously viewed topic.
- **Forward**—Displays the topic you viewed before clicking the **Back** button.
- **Options**—Displays a list of commands and viewing options for the help file.

Searching Help (Windows Only)

Use the **Search** tab to the left of this window to locate content in this help file. If you want to search for words in a certain order, such as "related documentation," add quotation marks around the search words as shown in the example. Searching for terms on the **Search** tab allows you to quickly locate specific information and information in topics that are not included on the **Contents** tab.

Wildcards

You also can search using asterisk (*) or question mark (?) wildcards. Use the asterisk wildcard to return topics that contain a certain string. For example, a search for "prog*" lists topics that contain the words "program," "programmatically," "progress," and so on.

Use the question mark wildcard as a substitute for a single character in a search term. For example, "?ext" lists topics that contain the words "next," "text," and so on.



Note Wildcard searching will not work on Simplified Chinese, Traditional Chinese, Japanese, and Korean systems.

Nested Expressions

Use nested expressions to combine searches to further refine a search. You can use Boolean expressions and wildcards in a nested expression. For example, "example AND (program OR VI)" lists topics that contain "example program" or "example VI." You cannot nest expressions more than five levels.

Boolean Expressions

Click the **•** button to add Boolean expressions to a search. The following Boolean operators are available:

- **AND** (default)—Returns topics that contain both search terms. You do not need to specify this operator unless you are using nested expressions.
- **OR**—Returns topics that contain either the first or second term.
- **NOT**—Returns topics that contain the first term without the second term.
- **NEAR**—Returns topics that contain both terms within eight words of each other.

Search Options

Use the following checkboxes on the **Search** tab to customize a search:

- Search previous results—Narrows the results from a search that returned too many topics. You must remove the checkmark from this checkbox to search all topics.
- Match similar words—Broadens a search to return topics that contain words similar to the search terms. For example, a search for "program" lists topics that include the words "programs," "programming," and so on.
- Search titles only—Searches only in the titles of topics.

Printing Help File Topics (Windows Only)

Complete the following steps to print an entire book from the **Contents** tab:

- 1. Right-click the book.
- 2. Select **Print** from the shortcut menu to display the **Print Topics** dialog box.
- 3. Select the **Print the selected heading and all subtopics** option.
 - Note Select Print the selected topic if you want to print the single topic you have selected in the **Contents** tab.
- 4. Click the **OK** button.

Printing PDF Documents

This help file may contain links to PDF documents. To print PDF documents, click the print button located on the Adobe Acrobat Viewer toolbar.

Fundamentals

Expand this topic for fundamental information about waveforms and video signals.

Waveform Fundamentals

Expand this topic for information about the fundamentals of waveforms.

Bandwidth and Passband Flatness

The *bandwidth* of a signal source is defined as the frequency at which the amplitude of the frequency response is 3 dB lower than the amplitude of the frequency response at DC or a low frequency. The bandwidth of a source is limited by the output amplifier design or by filters in the analog output circuit. Bandwidth is one of the factors that determines the capability of the source to create signals with specific frequency content.



Note On some NI signal generators you can enable or disable the filters.

Passband flatness is a measure of the amplitude accuracy of the frequency response with respect to frequency. Passband flatness is usually specified in ±dB, and it is usually referenced to the amplitude of the frequency response at a designated frequency.

For example, a specification might be listed as ± 1 dB with respect to the amplitude of the frequency response at 50 kHz. This method is used because two different metrology instruments, a digital multimeter (DMM) and a power meter, are used to measure passband flatness. The power meter is an excellent metrology instrument for measuring passband flatness, but its performance can be improved by calibrating its frequency response at a low frequency, such as 50 kHz, with a DMM. In other words, the DMM measures the amplitude of a 50 kHz tone, and the power meter measures the amplitude of all other frequencies with respect to the amplitude of the 50 kHz tone measured by the DMM.

Passband flatness is important in many applications. For example, if the sensitivity of a receiver is being tested, it is important to know the variation of the amplitude of the test tone as it is swept across the frequency band of interest. Some NI signal generators have a Direct Output analog path that has been optimized for passband flatness. Others allow you to select a frequency at which the calibrated amplitudes can be finely adjusted to achieve the best amplitude accuracy near the selected frequency.

Sample Rate

Sample rate is the rate at which digital data is transferred from the memory to the digital-to-analog converter (DAC). According to Shannon's Sampling theorem, a digital waveform must be updated at least twice as fast as the bandwidth of the signal to be accurately generated. Ideally, a sample rate many times greater than the frequency of the signal produces accurate waveforms. A higher sample rate also captures more waveform details. The following figure illustrates a 1 MHz sine wave generated by a sampled 2 MS/s DAC and a 20 MS/s DAC. The faster DAC generates 20 points per cycle of the expected signal compared with 2 points per cycle with the slower DAC. In this example, the higher sample rate more accurately defines the waveform shape.



Nyquist and Shannon's Sampling Theorems

The Nyquist theorem concerns digital sampling of a continuous time analog waveform, while Shannon's Sampling theorem concerns the creation of a continuous time analog waveform from digital, discrete samples.

Nyquist Theorem

The Nyquist theorem states that an analog signal must be sampled at least twice as fast as the bandwidth of the signal to accurately reconstruct the waveform; otherwise, the high-frequency content creates an *alias* at a frequency inside the spectrum of interest (*passband*). An alias is a false lower frequency component that appears in sampled data acquired at too low a sampling rate. The following figure shows a 5 MHz sine wave digitized by a 6 MS/s analog-to-digital converter (ADC). In this figure, the solid line represents the sine wave being digitized, while the dotted line represents the aliased signal recorded by the ADC at that sample rate.



The 5 MHz frequency aliases back in the passband, falsely appearing as a 1 MHz sine wave.

Shannon's Sampling Theorem

Shannon's Sampling theorem states that a digital waveform must be updated at least twice as fast as the bandwidth of the signal to be accurately generated. The same image that was used for the Nyquist example can be used to demonstrate Shannon's Sampling theorem. The following figure shows a desired 5 MHz sine wave generated by a 6 MS/s DAC. The solid line represents the desired waveform, and the arrows represent the digitized samples that are available to recreate the continuous time 5 MHz sine wave. The dotted line indicates the signal that would be seen, for example, with an oscilloscope at the output of a DAC.



In this case, the high–frequency sine wave is the desired signal, but was severely undersampled by only being generated by a 6 MS/s DAC; the actual resulting waveform is a 1 MHz signal.

In systems where you want to generate accurate signals using sampled data, the sampling rate must be set high enough to prevent aliasing.

Aliased Images

An aliased image is a frequency component that appears in continuous time waveforms being re–created from discrete–time, digital waveforms. The frequencies where these extra components appear are related to both the frequency of the signals being re–created as well as the frequency of the sample rate. Looking only at positive frequencies, the two frequencies are related by the following equation:

$$f_{ai} = |f_o + nf_s|$$

where

 f_{ai} = the aliased images

 f_o = the desired waveform frequency

 $f_{\rm s}$ = the sample rate

n = an integer (either positive or negative)

As the equation indicates, there are an infinite number of these aliased images that occur although. As *n* gets larger, however, the power content of these extra frequencies "falls off."

The following figure shows a 1 MHz sine wave generated by a 6 MS/s DAC. The dotted line represents an aliased image signal that shows up as a 5 MHz component. In this case, f_o is 1 MHz, n is –1, and f_s is 6 MHz; resulting in the following formula:

 $f_{ai} = 5 \text{ MHz} = |1 \text{ MHz} + (-1)(6 \text{ MHz})|$

The other possible frequencies of sine waves can be calculated and superimposed onto the sampling points of the image.



The following figure shows the frequency domain representation of the previous example. The vertical arrow at f_0 represents the frequency and signal power of the desired generated signal. The other vertical arrows represent the frequencies and signal powers of the aliased image

frequency components that appear in the frequency spectrum.



In systems where you want to generate accurate signals using sampled data, an optional lowpass filter must be introduced after the DAC to restrict the bandwidth of the output signal to meet the sampling criteria (<u>Shannon's Sampling theorem</u>). For more information about filtering, refer to <u>Filtering and Interpolation</u>.

DAC Resolution

Digital-to-analog converter (DAC) resolution is a limiting factor in determining the accuracy of the re-creation of an analog waveform from digital samples. More details are present in the waveform if the DAC resolution is increased. A 3-bit DAC divides its vertical range into eight discrete levels. With a vertical range of 10 V, the 3-bit DAC cannot generate voltage differences smaller than 1.25 V. In comparison, a 16-bit DAC with 65,536 discrete levels can generate voltage differences as small as 153 μ V.

The following figure shows the difference between two waveforms. The 16-bit waveform looks like a continuous sine wave, but if you were to zoom in, you would see the discrete steps of 153 μ V. Both waveforms are composed of discrete voltage steps, but the 16-bit version looks much closer to a "pure" continuous-time sine waveform.



Arbitrary Waveform Generation Mode

For NI signal generators, the Arbitrary Waveform Generation mode generates waveforms from user–created or user–provided waveform arrays of numeric data. The waveform arrays are downloaded to the onboard memory on the arbitrary waveform generator. Arbitrary Waveform Generation mode also uses memory for storing the instructions for generating waveform sequences in the waveform memory.

For more information about waveform generation, refer to <u>Standard</u> <u>Function Mode</u>.

Digital Pattern Generation

Some NI signal generators support 16-bit digital pattern generation at a digital connector. The digital pattern generation provides a digital representation of the waveforms generated on the analog connector of the device at the same rates as the analog signal.

Marker Output Signal

A marker is a digital pulse that NI signal generators can generate at specific points within a waveform generation. You can route this signal to connectors on the front panel or to PXI trigger lines or RTSI trigger lines depending on the device. You can place a marker in every sequence segment. A marker can be used as a trigger for controlling the timing of other devices in your application.

You can specify a marker by giving an offset count (in number of samples) from the start of the waveform buffer for each segment. If the waveform *loops* multiple times in a segment, the marker generates each time the waveform loops at the configured sample position.

If you need to generate a marker only once in a segment where the waveform loops a number of times, break the segment up into multiple segments. For example, if you need to generate a marker on only the first iteration of a sine waveform that loops 100 times, create a segment that generates the sine waveform with the marker at a specific sample position, and loops only once. Create a second segment that generates the sine waveform with no marker and loops 99 times.

This technique can be used in different combinations of segments to generate one marker every 10 of the sine waveform by creating a segment containing a marker and one loop followed by a segment with no markers that is looping nine times. These two segments are repeated as long as you need to repeat the cycle.

Minimum Waveform Size and Quantum

The memory architecture of the NI signal generators imposes certain requirements on the waveform size and quantum. If these requirements are not met, NI-FGEN returns an error. The specific values for minimum waveform size and quantum depend on the specific NI signal generator being used.

Minimum Waveform Size

Every waveform downloaded to the device memory must be at least a minimum size in terms of the number of samples.

Quantum

The size in samples of the waveform downloaded to the device memory must be an integer multiple of a certain number or quantum.

For example, if the minimum waveform size for a particular signal generator is 256 samples, the quantum is eight samples, and you request to load a waveform of 255 samples, NI-FGEN returns an error because the waveform size is too small. If you request to load a waveform of 257 samples, NI-FGEN also returns an error because even though the size is larger than the minimum waveform size, the waveform is not an integer multiple of the quantum size (8).

Waveform sizes that meet the restrictions for this example include 256, 264, 272, and 280 samples, and so on—up to the actual device memory size.

Standard Function Mode

Standard Function output mode is used to generate standard function waveforms such as sine, square, triangle, and so on.

NI 5401/5402/5406/5411/5431/5441/5442

For the NI 5401/5402/5406/5411/5431/5441/5442, the Standard Function mode is implemented through <u>direct digital synthesis</u> (DDS), which is a technique for deriving, under digital control, an analog frequency source from a single Reference clock frequency. This technique produces high-frequency accuracy and resolution, temperature stability, wideband tuning, and rapid, phase-continuous frequency switching.

In DDS mode, a fixed–size memory (called *lookup memory*) stores one cycle of a periodic waveform. A phase accumulator indexes the lookup memory. For each cycle of the device Sample clock, the sample of the waveform in lookup memory that is addressed by the phase accumulator is returned. The accumulator is then incremented by the value in the frequency control word (FCW). By adjusting the <u>Frequency</u> property or the <u>NIFGEN ATTR FUNC FREQUENCY</u> attribute, NI-FGEN calculates the corresponding FCW, and you can vary the output frequency of the waveform in lookup memory. The phase accumulator increments in smaller steps for smaller FCWs. Accordingly, you need more samples to generate one waveform cycle, so the frequency is lower. A higher FCW results in a higher frequency. In DDS mode, the Sample clock does not vary with the frequency of the generated waveform. At higher frequencies, some waveform samples in lookup memory are skipped; at lower frequencies, some samples output multiple times in succession.

NI 5412/5421/5422

For the NI 5412/5421/5422, the Standard Function output mode is implemented primarily in software. Instead of using separate DDS hardware to generate standard function waveforms, NI-FGEN creates and downloads standard function waveforms to arbitrary waveform memory and generates them just like arbitrary waveforms. NI-FGEN automatically selects the best clock mode, sample rate, and buffer size to produce the most accurate waveform possible. To determine how much arbitrary memory is used, query the <u>Buffer Size</u> property or the <u>NIFGEN_ATTR_FUNC_BUFFER_SIZE</u> attribute. To adjust the maximum amount of memory used by NI-FGEN for generating standard function waveforms, set the <u>Max Buffer Size</u> property <u>NIFGEN_ATTR_FUNC_MAX_BUFFER_SIZE</u> attribute. Increasing the maximum buffer size may result in a more accurate waveform.

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Note <u>Frequency hopping and sweeping</u> is not supported on the NI 5412/5421/5422.

Waveform Fundamentals Direct Digital Synthesis

The <u>Standard Function mode</u> is implemented through direct digital synthesis (DDS).

The following figure shows the building blocks for DDS-based waveform generation.



You can use the <u>lookup memory</u> in Function Generation mode only. You cannot use the lookup memory in <u>Arbitrary Waveform Generation mode</u>. You can store one cycle of a repetitive waveform—a sine, triangular, square, or arbitrary wave—in the lookup memory. Then, you can change the frequency of that waveform by sending just one instruction. You can use Function Generation mode for very fine frequency resolution function generation. Because Function Generation mode uses an accumulator, waveform generation loops back to the beginning of the lookup memory after passing through the end of the lookup memory.

In Function Generation mode, each stage is made up of two instructions: the frequency and the time. The frequency instruction specifies the frequency of the waveform generation. The time instruction specifies the amount of time that the frequency generates.



Note You cannot specify the number of iterations for a waveform to generate in Function Generation mode.

Frequency Hopping and Sweeping

You can define a staging list for performing frequency *hops* and *sweeps*. The entire staging list uses the same waveform loaded into the lookup memory. All stages are phase-continuous and differ only with the frequency generated.

Frequency Sweeping

A frequency sweep is the continuous generation of a single waveform with a linearly-changing frequency.

The following are the basic elements used to control the generation of a frequency sweep:

- Start Frequency—the first frequency generated in the frequency sweep.
- End Frequency—the last frequency generated in the frequency sweep.
- Number of Frequency Steps—the number of segments into which a waveform is divided. Each frequency step corresponds to a particular frequency.
- Frequency Step Duration—the amount of time the waveform is generated at a particular frequency.

These elements can be used to programmatically create a frequency sweep. Refer to niFgen_Sweep_Generator_Example or niFgen_5404_Frequency_Sweep_Example for LabVIEW, or Sweep Generator or 5404 Frequency Sweep for LabWindows/CVI for an example of how this is accomplished.

A simple example of a frequency sweep is a chirp waveform—a sine wave produced with a linear sweep of frequency. Refer to the <u>NI Analog</u> <u>Waveform Editor Help</u> for information about creating and configuring a chirp waveform using the AWE.
Frequency Hopping

Frequency hopping is similar to frequency sweeping, with the difference that the frequencies used in a frequency hop are not applied in a linear succession, but rather in an order defined by the user. You can use Frequency List mode, Sequence mode, or Script mode to implement frequency hopping.

Clocking

Divide-Down Clocking

Divide-down clocking uses the Sample Clock Timebase—the main timing component—of the device. This component is usually a voltage—controlled crystal oscillator (VCXO). The valid sample rates for divide-down clocking are integer divisions of the Sample Clock Timebase frequency. The sample rate is given by the formula:

SR = SCTF/n

where

SR = sample rate

n = integer from 1 to a maximum value for the specific device

SCTF = Sample clock timebase frequency for the specific device

For example, for a signal generator with a Sample clock timebase frequency of 100 MS/s, SCTF = 100 MS/s, and the available sample rates are integer divisions of 100 MS/s, as shown in the following examples:

SCTF/1 = 100 MS/s SCTF/2 = 50 MS/s SCTF/3 = 33.333 MS/s

As the integer *n* increases, the available sample rate decreases. If you choose a sample rate other than an integer division of the Sample clock timebase, the device usually coerces the sample rate setting to the nearest sample rate or integer division of the Sample clock timebase.

Divide-down clocking provides the lowest jitter Sample clock, and is also referred to as */N* or divide by *n* clocking.

High-Resolution Clocking

High-resolution clocking allows you to set the Sample clock frequency to any value from zero to the device Sample clock timebase frequency with a very fine resolution typically in the millihertz or microhertz range. This mode is useful for applications that require a precise clock source, which is not possible using the divide-down clocking scheme.

High-resolution clocking has more jitter than divide-down clocking.

External Clocking

External clocking allows you to connect an external clock to the NI signal generator. This external clock can then be used as the Sample clock for the device.

Impedance Matching

When broadband signals are carried on transmission lines of any significant length, care must be taken that the transmission line is matched to its terminations. The source and load impedances should equal the characteristic impedance of the transmission line, as this minimizes signal reflections. The presence of impedance discontinuities or mismatches degrade the amplitude and phase accuracy, as well as the temporal fidelity, of waveforms generated with a signal generator.

One of the most common mismatch errors encountered in such measurements is shown in the following figure:



In this example, selectable source impedances are provided at the signal generator outputs to accommodate the most popular coaxial cable characteristic impedances: 50 Ω and 75 Ω . The following figure shows what happens when, as in this example, a coaxial cable of the wrong characteristic impedance (50 Ω) is used with 75 Ω source and load impedances:



The pulse encounters impedance mismatches at each end of the cable, causing the pulse to be partially reflected. The reflected pulse traverses the cable back and forth numerous times, diminishing at each end by the reflection coefficient, $_{\Gamma}$.

$$\Gamma = \frac{v_r}{v_i} = \frac{z_t - z_0}{z_t + z_0}$$

where

 v_r = reflected voltage

 v_i = incident voltage

 z_t = terminating impedance

 z_0 = characteristic impedance

The resulting voltage waveform is distorted by the asymptotic decay of the reflected pulse as shown, exaggerated for visual effect. Impedance discontinuities of smaller magnitude and/or duration have correspondingly smaller effects. Also displayed is the waveform that results when a cable of matched impedance (75 Ω) is used.

Mismatch Uncertainty

Impedance matching is also important for preserving the absolute delivered power from a device. The accuracy with which power can be delivered is limited by mismatch error. The mismatch error in a z_0 system can be shown to be bounded by:

$$\frac{\left(1 - |\Gamma_{\mathcal{I}}|^{2}\right)}{\left(1 + |\Gamma_{\mathcal{I}}| \cdot |\Gamma_{\mathcal{G}}|\right)^{2}} \leq \text{mismatch error} \leq \frac{\left(1 - |\Gamma_{\mathcal{I}}|^{2}\right)}{\left(1 - |\Gamma_{\mathcal{I}}| \cdot |\Gamma_{\mathcal{G}}|\right)^{2}}$$

$$\Gamma_{\mathcal{I}} = \text{load reflection coefficient}$$

 Γ_{G} = generator reflection coefficient

The denominator term represents mismatch uncertainty, which is a fundamental limit to the power transfer accuracy that can be achieved across a mismatched junction.

Resistive Matching

Signal generators with low/high-source impedance can be matched with a resistor placed in series (shunt) such that the total source impedance (admittance) is matched to the cable characteristic impedance (admittance). Signal generators that are not capable of driving the cable impedance directly can be coupled through a matching L-pad. In this case, the signal generator sees an approximately 500 Ω load, while the source impedance presented to the cable is 50 Ω , as shown in the following figure:



High-frequency components and layout techniques should be used throughout to minimize parasitic effects.

Output Attenuation

Output attenuation is a method of controlling the output voltage level of the signal being generated. NI signal generators typically generate signals with a digital-to-analog converter (DAC) that has an output voltage range of -5.0 V to +5.0 V with a number of bits of resolution. This signal is applied to an attenuator that controls the output voltage of the signal source.

By attenuating the DAC output signal, you keep the dynamic range of the DAC; that is, you do not lose any bits from the digital representation of the signal because the attenuation is done after the DAC and not before it.

For example, if a DAC with a range of -5.0 V to +5.0 V and a resolution of 12 bits with each bit corresponding to 2.44 mV [(+5.0 - (-5.0)) / 2^12] does not use output attenuation, and the desired signal is 2.0 V_{pk-pk} (- 1.0 V to +1.0 V), waveform values can be generated with the DAC that only use $^{1}/_{5}$ of the DAC range. The resolution of each digital bit is still 2.44 mV.

However, if the same DAC uses the output attenuation, the full range of the DAC generates the signal, creating the signal at the full 10.0 V_{pk-pk}. The value of each digital bit is still the original 2.44 mV. The signal is applied to an attenuator, which reduces the voltage level by a factor of 5 to 2.0 V_{pk-pk}. The attenuator also reduces the value of each bit, which results in an effective bit value of 0.488 mV at the analog output connector. The attenuator allows the use of the full range of the DAC, and reduces the effective value of each bit corresponding to the degree of attenuation.

Output Enable

You can switch off the waveform generation at the output connector by controlling the output enable relay on select devices. When the output enable relay is off, the output signal level goes to ground level.

Output Impedance

NI signal generators have an output impedance of 50 Ω and an optional 75 Ω on select devices.

If the load impedance matches the output impedance, the voltage at the signal output connector is at the needed level. The voltage at the signal output connector varies with load output impedance, up to doubling the voltage for a high impedance load, as shown in the following figure.



In the previous figure, the required output voltage is ± 5 V. The NI signal generator internal voltage source generates twice this voltage, ± 10 V, expecting the voltage to be halved due to the voltage divider formed by R_O and R_L . The relationship between the output voltage and the load can be calculated as follows:

 $V_{out} = [R_L/(R_L + R_O)] \times [V_S]$

where

 V_{out} = the voltage level delivered to R_L

 R_L = the load impedance in ohms

 R_O = the output impedance on the NI signal generator

 $V_{\rm S}$ = the voltage level generated by the source previous to $R_{\rm O}$

By default, $R_O = 50 \Omega$, but you can use NI-FGEN to set it to 75 Ω on select devices. Also, with some devices you can enter the value of R_L , and the device changes V_S accordingly to deliver the requested V_{out} .

Phase-Locked Looping

A phase–lock loop (PLL) is a circuit that adjusts a main clock to synchronize to a Reference clock. The frequency stability of the Sample clock timebase matches that of the Reference clock when the two are phase–locked. Phase locking also synchronizes clocks of multiple devices that are phase–locked to the same Reference clock.

The following figure shows a block diagram of a basic PLL.



The operation of this circuit is typical of all PLLs. A PLL is a feedback control system that controls the phase of a voltage–controlled oscillator (VCO). The frequency reference signal is applied to a phase detector. The output of the VCO connects to the other input. Normally the frequencies of both signals are almost the same. The output of the phase detector has a voltage proportional to the phase difference between the two input signals. The loop filter receives this signal from the phase detector. The loop filter determines the dynamic characteristics of the PLL.

Triggering

Triggers are signals that cause the NI device to perform an action such as starting or stopping a generation operation. Triggers can be internal (software-generated) or external. External digital triggers can be several different types. External triggers can be re-exported and, along with events, can allow you to synchronize the hardware operation with external circuitry or other NI devices.

Refer to <u>Triggers Summary</u> and <u>Events</u> for descriptions of the triggers and events you can use with your device.

When triggering your NI signal generator, you can select the <u>type of</u> <u>trigger</u>, the <u>trigger source</u>, and the <u>trigger mode</u> that you want to use.

Triggers Summary

The following table describes the triggers supported by signal generators. The *Supported Types* column denotes which trigger types are valid for a given trigger.

Trigger Name	Supported Types	Description
Start	<u>Digital</u> <u>Edge,</u> Software	The Start trigger transitions a device from an idle state to a generation state where the device can respond to Sample clocks.
Script	<u>Digital</u> <u>Edge,</u> <u>Digital</u> <u>Level,</u> <u>Software</u>	The Script trigger is a general-purpose trigger with a role that is entirely determined by the context of the generation script. A <u>script</u> allows you to create sophisticated generation operations. For example, the script could configure the device to generate waveform A, then wait for the Script trigger, then generate waveform B. You can create multiple Script triggers for use in your application.
		Once a digital edge Script trigger has been received, that trigger remains true for all subsequent instructions until the <u>clear</u> instruction is called or the trigger is reset after being used in the <u>wait</u> , <u>repeat/end repeat</u> , or <u>if</u> instructions.

Types of Triggers

A trigger is an external stimulus that initiates one or more device functions. Trigger stimuli include digital edges, software functions, and analog levels.

You can trigger your NI signal generator with one of the following types of triggers:

- Edge
- Level
- <u>Software</u>

Note Individual triggers may not support all the trigger types listed here. Refer to <u>Triggers Summary</u> for more information.

Edge Trigger

A digital signal has two discrete levels: a high level and a low level. When the signal transitions from high to low or from low to high, a *digital edge* is created. There are two types of edges: rising, which occurs when the signal transitions from low level to high level, and falling, which occurs with a transition from high level to low level. Triggers configured to act on a rising or falling edge of a digital signal are called *edge triggers*.

As the following figure shows, an edge trigger could be configured to occur either at the place labeled *Falling Edge of Signal* or at *Rising Edge of Signal*.



Level Trigger

You can configure certain triggers to act when a signal goes below the defined low level or above the defined high level. Triggers configured to act in this way are known as *level triggers*. Not all triggers can be configured to be level triggers. Refer to <u>Triggers Summary</u> for information about which triggers you can configure for level triggering.

Software Triggers

A software trigger is generated internally by a programmatic call to the <u>niFgen Send Software Edge Trigger</u> VI or the

<u>niFgen_SendSoftwareEdgeTrigger</u> function and can occur at any time, based upon the conditions specified in the program.

Trigger Modes

Frequency List, Arbitrary Waveform, and Arbitrary Sequence output modes support multiple trigger modes that affect the behavior of the signal generator when receiving triggers. These trigger modes include Single trigger mode, Continuous trigger mode, Stepped trigger mode, and Burst trigger mode. Refer to the output mode for more information about triggering behavior.



Note Not all trigger modes are available on all NI signal generators. Refer to the device-specific topics for information about which trigger modes are available for your signal generator.

Trigger Sources

Possible trigger sources include the following:

- Immediate
- Digital front panel connector
- RTSI bus trigger lines (PCI devices)
- PXI trigger bus lines (backplane of PXI devices)
- PXI Star trigger line
- PFI inputs (SMB front panel connectors)

The following figure shows the trigger sources for NI signal generators.



For NI signal generators, trigger sources are software selectable. To set a trigger source, use the parameters in <u>niFgen_ConfigureTriggerSource</u>.

Events

An event is a signal generated by the NI device at a device state. Typically, events are configured to indicate when a specific hardware condition has been met. Refer to <u>Features Supported</u> to determine what events your signal generator supports.

Event Output Behaviors

Events can have one of three output behaviors. Refer to the following table to determine which output behaviors are supported by each event.

- Toggle—Each instance of the event toggles between high and low. You can set the initial state of the event.
- Pulse—Each event triggers a pulse for a specified period of time.
- Level—While the event is active, it shifts high or low depending on the active state you specify.

Event Status

Events can return their status in two ways. Refer to the following table to determine what status can be read for each event type.

- Live—Returns the current state of the event.
- Latched—Returns whether the event has ever been active.

The following table describes the event output behaviors and statuses supported by NI signal generators:

Event Name	Description	Output Behavior	Status
Ready for Start Event	Ready For Start event indicates that the signal generator is configured and ready to receive a Start trigger.	Level	Live
Started Event	Started event indicates when the signal generator has received a Start trigger and is generating a waveform.	Level, Pulse	Latched
<u>Marker</u> Event	A Marker is an event that the device generates in relation to a waveform that is generated. The event is configured to occur at the time that a specific location or sample <i>n</i> if the waveform generates on the CH 0 connector. If the waveform loops multiple times in a segment, the marker generates each time the waveform loops.	Pulse, Toggle	Latched, Live
<u>Data</u> <u>Marker</u> <u>Event</u>	A Data Marker is an event that the signal generator generates in relation to the data bits of a waveform that is generated. Up to four bits can be configured to export to any valid destination on the signal generator.	Level	N/A
Done Event	The Done event indicates that the generation of the previous waveform is complete.	Level, Pulse	Latched

Event Delays

NI 5402/5406/5412/5421/5422/5441/5442 devices support event delays that can manually delay Marker, Started, and Done events so that they are aligned on a particular Sample clock period. For more information about event delays, refer to the <u>Event Delays</u> topic.

Marker Events

A marker is an event that the device generates in relation to a waveform that is generated. The event is configured to occur at the time that a specific location or sample *n* in the waveform generates on the CH 0 connector. If the waveform loops multiple times in a segment, the marker generates each time the waveform loops. The following figure shows a pulse that represents a waveform sample *n* that is one Sample clock in width of a waveform being generated on the CH 0 connector. The second pulse, the Marker event, represents the pulse that generates when the corresponding waveform sample *n* outputs at the CH 0 connector. Refer to Features Supported to determine if your device supports markers.



 t_{m1} represents the delay in time of the Marker event generated relative to the configured waveform sample *n* being generated.

 t_{m2} represents the Marker event pulse width in time.

NI-FGEN takes into account the factors that affect the delays in the Digital and Analog paths in assuring that the Marker event appears within one Sample clock of the waveform output. Therefore, t_{m1} is less than one Sample clock period.

The Marker event pulse width, t_{m2} , is at least 150 ns and can be significantly longer than 150 ns for slower Sample clocks. You can configure the pulse width by setting the <u>Marker Event Pulse Width</u> property or the <u>NIFGEN ATTR MARKER EVENT PULSE WIDTH</u> attribute. Instruments commonly have a minimum pulse width specification for a trigger to be registered, and trigger pulses of smaller width are ignored. The signal generator ensures that a minimum pulse width exists on the Marker event by using a pulse stretching circuit. A Sample clock rate of 100 MS/s has a period of 10 ns, requiring the pulse to be lengthened for many devices to register the marker as a good trigger pulse. Refer to the <u>module specifications</u> for the timing specifications.

Creating Markers

You can specify a marker and its location by setting an offset location value (in number of samples) from the start of the waveform. If the offset is out of range of the number of samples in that segment, NI-FGEN returns an error. There are two rules for marker placement:

- 1. A marker can be specified only at offsets that are multiples of four samples (or two complex samples).
- 2. A marker must be placed at least four samples from the end of the waveform. In Burst trigger mode, a marker must be placed at least eight samples from the end of the waveform.

For example, for a waveform containing 100 samples, a marker at an offset of 0 or 4 is valid, but a marker at an offset of 3 is invalid. In addition, a marker at an offset of 97 or 100 is always invalid, while a marker at an offset of 96 is valid for all trigger modes except Burst. The marker can be placed at an offset of 92 for all trigger modes.

To create a marker in <u>Arbitrary Waveform Mode</u>, set the <u>Arbitrary</u> <u>Waveform Marker Position</u> property or the <u>NIFGEN_ATTR_ARB_MARKER_POSITION</u> attribute. Then use the <u>niFgen Export Signal</u> VI or the <u>niFgen_ExportSignal</u> function to export the marker signal.

To create a marker in <u>Arbitrary Sequence Mode</u>, refer to the **Marker Location Array** parameter of the <u>niFgen Create Advanced Arb</u> <u>Sequence</u> VI or the <u>niFgen_CreateAdvancedArbSequence</u> function. Then use the niFgen Export Signal VI or the niFgen_ExportSignal function to export the marker signal.

In <u>script mode</u>, you can create up to four markers for each waveform. To create markers in script mode, refer to the *NI Script Editor Help*. Then use the niFgen Export Signal VI or the niFgen_ExportSignal function to export the marker signal.



Note When exporting markers in script mode, you must specify the marker using the **Signal Identifier** parameter of the niFgen Export Signal VI or the niFgen_ExportSignal function.

Markers as Trigger Outputs

A delay of at least 44 Sample clocks exists between the Start trigger and the analog waveform generation on the output connector. Therefore, synchronizing the signal generator output signal to other devices with fast trigger response times is accomplished using the Marker event from the signal generator as the trigger source for the other device for more precise alignment to the generating waveform. You can do this using the RTSI bus, PXI trigger lines, SYNC OUT/PFI 0 and PFI 1 or PFI 4 and PFI 5. Refer to Exporting Signals for more information about routing signals off the device.

Note Devices without a DDC connector do not support PFI<4..5>.

Data Marker Events

The Data Marker events allow you to export any one of the 16 waveform data bits to any valid destination on the device. Up to four of the 16 waveform data bits can be exported at one time. Refer to <u>Features</u> <u>Supported</u> to determine if your device supports data marker events.

The level of a Data Marker event changes at the time that a specific data bit toggles in the waveform data. If the waveform data bit toggles multiple times in a segment, the Data Marker event level changes each time. When the data bit level is high, the Data Marker event level is high. You can invert this relationship by setting the <u>Data Marker Event Level</u> <u>Polarity</u> property or the

NIFGEN_ATTR_DATA_MARKER_EVENT_LEVEL_POLARITY attribute.

The following figure shows the exported data marker event shifting between low and high as the specified data bit toggles.



NI-FGEN compensates for the factors that affect the delays in the digital and analog paths in assuring that the Data Marker event appears within one Sample clock of the waveform output.

Creating and Exporting Data Marker Events

To create and export a Data Marker event, complete the following steps:

- Specify a data bit number using the <u>Data Marker Event Bit</u> <u>Number</u> property or the <u>NIFGEN_ATTR_DATA_MARKER_EVENT_DATA_BIT_NUMBER</u> attribute.
- 2. Set the output polarity of the data marker event using the Data Marker Event Level Polarity property or the NIFGEN_ATTR_DATA_MARKER_EVENT_LEVEL_POLARITY attribute.
- 3. To export the data marker, use the <u>niFgen Export Signal</u> VI or the <u>niFgen ExportSignal</u> function. To determine all possible signal routes for your device, refer to <u>Signal Routing</u>.
 - Note When exporting data markers, you must specify the signal identifier for the data marker using the of the niFgen Export Signal VI or the niFgen_ExportSignal function.

Data Markers as Trigger Outputs

A delay of at least 44 Sample clocks exists between the Start trigger and when the analog waveform generation on the output connector. Therefore, synchronizing the signal generator output signal to other devices with fast trigger response times is accomplished using the data marker event from the signal generator as the trigger source for the other device for more precise alignment to the generating waveform. You can do this using the RTSI bus, PXI trigger lines, SYNC OUT/PFI 0 and PFI 1 or PFI 4 and PFI 5. Refer to Exporting Signals for more information about routing signals off the device.

Note Devices without a DDC connector do not support PFI <4..5>.

Waveform Fundamentals Scripts

You can link and loop multiple waveforms together in a generation operation using a *script*. A script is a series of instructions that indicates how waveforms saved in the onboard memory should be sent to the DUT. The script can specify the order in which the waveforms are generated, the number of times they are generated, and the triggers and markers associated with the generation.

You can create a script to manage waveform generation based on multiple waveforms and triggers. For example, you could download waveforms A, B, C, and D into device memory. You could then write a script that would wait for a trigger to initiate generation and, upon receiving this trigger, generate waveform A three times with a marker at position 16 each time and finally generate waveforms B, C, and D twice (BCDBCD). The following is the script of this example:

```
script myFirstScript
wait until scriptTrigger0
repeat 3
generate waveformA marker0(16)
end repeat
repeat 2
generate waveformB
generate waveformC
generate waveformD
end repeat
end script
```

Related Topics:

- <u>Script Mode</u>
- <u>Common Scripting Use Cases</u>
- <u>Scripting Instructions</u>

Streaming

Streaming is a way to generate waveforms that are too large to fit in the onboard memory of the signal generator. Streaming can be used in <u>Arbitrary Waveform</u>, <u>Arbitrary Sequence</u>, or <u>Script</u> output modes.



Note Streaming is supported on NI 5421/5422/5441/5442 signal generators.

To stream waveform data, allocate and identify all or a portion of the signal generator onboard memory to act as an onboard waveform for streaming. Before initiating waveform generation, fill that onboard memory with the first part of your waveform. As the waveform is generated, space in the onboard memory becomes free and fill that space with new waveform data. Repeat the process of filling the freed onboard memory in blocks of new waveform data until the waveform is complete.

Streaming Waveform Data

The following instructions are a guide for configuring your application for streaming. For a programmatic example, refer to Fgen Arb Waveform Streaming.vi for LabVIEW or ArbitraryWaveformStreaming.prj for LabWindows/CVI.

As an example, we have a 1.6 GB waveform we want to generate and an NI 5421 signal generator with 256 MB of onboard memory. This 1.6 GB waveform may be in the host memory, on disk, or data that your application generates dynamically during generation.

~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	$\sim$	1.6 GB Waveform
		256 MB Onboard Memory of NI 5421

1. Specify the amount of onboard memory to be used for streaming.

Use the <u>niFgen Allocate Waveform</u> VI or the <u>niFgen_AllocateWaveform</u> function to specify the amount of onboard memory to reserve for streaming. The allocated memory, known as the streaming waveform, serves as a buffer for the streaming process. The size of the waveform you wish to stream must be evenly divisible by the amount of onboard memory allocated for streaming to prevent the streaming waveform from being overwritten before it has generated.

······································	1.6 GB Waveform
160 MB	160 MB Allocated for Streaming
	Remaining Onboard Memory Used for Additional Waveforms and Script Instructions

2. Identify the streaming waveform.

Set the <u>Streaming Waveform Handle</u> property or the <u>NIFGEN_ATTR_STREAMING_WAVEFORM_HANDLE</u> attribute to the waveform handle returned in Step 1. Setting this property or attribute ensures that none of your streaming data is overwritten before it is generated. NI-FGEN monitors your progress to ensure that you write fresh data fast enough to keep up with the generation. If your application fails to keep up or attempts to write fresh data over data that has not been generated, NI-FGEN returns an error.

$\sim$	$\sim$	$\sim$	$\sim \sim \sim$	$\sim\sim\sim$	$\sim$	1.6 GB Wave
	Set the s to Identif	Streamin y the Wa	g Waveform H weform for Str	andle Prop saming	erty	
	¥					
		160	MB			
	~~~~	~~~~	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	~~~~		
\sim	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	~~~	~~~~~	~~~~		

3. Fill the streaming waveform with initial data.

Call the <u>niFgen Write Waveform</u> VI or the <u>niFgen_WriteWaveform</u> function to write the first part of the waveform data to the streaming waveform in onboard memory.

- **Tip** When transferring large blocks of waveform data, break the data into smaller blocks and call the niFgen Write Waveform VI or the niFgen_WriteWaveform function multiple times. The data is appended sequentially. A computer can allocate smaller blocks of a large waveform faster than allocating a single large contiguous block in memory. Depending on the amount of RAM on the computer, transferring ten 16 MB blocks may be faster than transferring one 160 MB block.
- **Tip** NI-FGEN requires the quotient of the waveform size divided by the data transfer block size to be an integer value. If the waveform size is not an integer multiple of the block size, change either the waveform size or the block size. A fractional number of data blocks in the waveform returns an error message.

~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	1.6 GB Wavefor
Write First Portion to Onboard Memory	
160 MB	]
y www.ww	2
	Write First Portion to Onboard Memory

4. Begin generating the waveform.

Call the <u>niFgen Initiate Generation</u> VI or the <u>niFgen InitiateGeneration</u> function to begin the waveform generation. As the waveform generates, space in the streaming waveform becomes free.

mmmmmmmmmmmmmmmmmmmmmmmmmmmmmmmmmmmmmm	1.6 GB Waveform
As Waveform is Generated, Onboard Memory Becomes Free	
160 MB	

5. As the waveform generates, monitor available memory.

Use the <u>Space Available in Streaming Waveform</u> property or the <u>NIFGEN_ATTR_STREAMING_SPACE_AVAILABLE_IN_WAVEFOR</u> attribute to determine how much of the streaming waveform is free for writing new data. As the waveform generates, space becomes available to write more waveform data. After a certain amount, say 10 percent, of the allocated onboard memory becomes available, you can write a block of waveform data to the streaming waveform in onboard memory.

**Note** The Space Available in Streaming Waveform property ( NIFGEN_ATTR_STREAMING_SPACE_AVAILABLE_IN_WAVE) attribute specifies the total amount of space available in the streaming waveform. During generation, this available space r be in multiple locations with, for example, part of the available
at the end of the streaming waveform and the rest at the begir In this situation, writing a block of waveform data the size of th space available in the streaming waveform causes NI-FGEN to return an error, as NI-FGEN will not wrap the data from the enthe waveform to the beginning and cannot write data past the the waveform buffer.

To avoid writing data past the end of the waveform, write new to the waveform in a fixed size that is an integer divisor of the size of the streaming waveform.

······	1.6 GB Waveform
Query the Space Available in Streaming Waveforr Property to Determine Freed Onboard Memory	n
160 MB	

6. Write a block of waveform data.

Call <u>niFgen Write Waveform</u> VI or the <u>niFgen_WriteWaveform</u> function to write a new block of waveform data to the streaming waveform in onboard memory.

16 MB	
↓	
	1.6 GB Waveform
Write Waveform Data in Blocks	
▼ 160 MB	

7. Repeat the process of monitoring the available memory and writing waveform data in blocks as free space becomes available.



### **Average Performance Rates**

The following tables list the average data rates possible for PXI, PCI, and PXI Express signal generators. Average data transfer rates are highly system dependent. The following table is intended to give you an idea of the average sustainable transfer rates using 16-bit (or 2 byte) samples.

### PXI and PCI

Data Source	Data Rate ¹		
Data Source	MS/s	MB/s	
Host memory on desktop computer or PXI embedded controller	~45 to 47.5	~90 to 115	
Desktop IDE or SATA hard drive	~27.5 to 35	~55 to 70 <mark>2</mark>	
Laptop or low RPM hard drive	12.5 to 15	25 to 30 <mark>2</mark>	
Host memory on desktop across MXI-3 to PXI board	12.5	25	
Host memory on desktop across MXI-4 to PXI board	12.5	25	
¹ All data rates highly dependent on chipset.			

² Measurements were taken using the Windows API for unbuffered file I/O.

For more information, refer to <u>High Speed Streaming Solutions</u>.

### **PXI Express**

Data Source	Data Rate ¹	
Dala Source	MS/s	MB/s
Host memory on desktop computer or PXI embedded controller	~262	~524
Desktop IDE or SATA hard drive	~155	~310
¹ All data rates highly dependant on chipset.		

Note These numbers were obtained using several file I/O optimizations. For more information about this streaming process, refer to <u>High Speed Streaming Solutions</u>.

### **Improving Streaming Performance**

To improve your maximum sustainable transfer rate for streaming, consider the following recommendations:

- Adjust the Data Transfer Block Size property or the <u>NIFGEN_ATTR_DATA_TRANSFER_BLOCK_SIZE</u> attribute. The default data transfer block size for NI-FGEN is 2 MS (or 4 MB). If you were to write a 16 MB waveform to the signal generator, the complete transfer would occur using four separate DMA transfers. If you modify the data transfer block size to 8 MS (16 MB), for example, the data transfer is more efficient and is instead accomplished in a single transfer.
- When streaming from hard drives, consider the hard drive speed for maximum sustainable rates. Laptop hard drives typically have a data transfer rate of 5 to 10 MB/s. Desktop hard drives often can meet 20 MB/s.

Transfer rates from hard drives can vary for a number of reasons, including where the data is physically stored on the hard drive and how much data is stored. Storing your waveform files on a fairly empty, defragmented hard drive may help increase performance.

- Consider using a RAID (redundant array of independent disks) configuration to utilize striping to increase data transfer rates from disk.
- When using 18-slot PXI chassis, install the signal generator used for streaming in the first segment (Slots 2 to 6) of the PXI chassis.
- Utilize <u>Direct DMA</u>.

## Waveform Fundamentals Direct DMA

Direct DMA can be used to transfer waveform data to the signal generator onboard memory at rates well beyond the typical 5 to 30 MB/sec range in a standard PC-based architecture. To achieve such high rates, Direct DMA establishes a direct connection between the signal generator onboard memory and a specialized waveform data source. Direct DMA is commonly used to <u>stream</u> waveform data from disk at data rates of greater than 100 MB/s.

In a standard PC-based architecture playback rates to the 5 to 40 MB/sec range are limited by the following factors:

- Shared data paths through the PCI controller, I/O bus, CPU, and memory that divide down bandwidth
- Latencies introduced by the operating system and application software managing data flow
- Non-deterministic operating system management of file I/O

For example, in a standard PC-based architecture, downloading a waveform to the onboard memory of your signal generator requires the following process for every 4,096 byte segment of physical memory:

- 1. The signal generator retrieves an address identifying the location of the data segment in the host memory.
- 2. The signal generator uses the address to request transfer of the data segment in the host memory.
- 3. The signal generator downloads the data to the onboard memory of the signal generator.
- 4. Steps 1-3 repeat every 4,096 bytes until the waveform data is fully downloaded.

To download a 16 MB waveform (16,777,216 bytes), this process repeats 4,096 times (16,777,216 bytes/4,096 bytes).

The direct connection established by Direct DMA to the data source is able to minimize or eliminate the factors that limit playback rates. To download data to the onboard memory of the signal generator with Direct DMA, the following process occurs only once:

1. The signal generator retrieves an address identifying the location

of the waveform data source. This address generally refers to a large window of physically contiguous memory.

- 2. The signal generator uses the address to contact the waveform data source.
- 3. The signal generator requests the data segment and size from waveform data source. In this case, the size requested by the signal generator can be fairly large (for example, 16 MB).
- 4. The signal generator downloads the data to the onboard memory of the signal generator from the waveform data source in one operation.

The transfer process is much faster and more efficient because an address to the waveform data is requested once (in this case, the address is to the waveform data source).

### **Related Topics**

• Configuring Direct DMA.

## Waveform Fundamentals Frequency Domain Fundamentals

Expand this book to view the frequency domain topics, or click one of the following links:

- <u>SFDR</u> Spurious–free dynamic range
- THD Total harmonic distortion
- <u>SINAD</u> Signal-to-noise-and-distortion ratio
- **ENOB** Effective number of bits

# SFDR

Spurious–free dynamic range (SFDR) is the usable dynamic range before spurious noise interferes with or distorts the fundamental signal. For specification purposes, the amplitude of the fundamental signal is usually –1 dBFS. SFDR is the measure of the difference in amplitude between the fundamental signal and the largest harmonically or nonharmonically related spur from DC to the full <u>Nyquist</u> bandwidth (half the sampling rate). A spur is any frequency bin on a spectrum analyzer, or from a Fourier transform, of the analog signal. SFDR is expressed in dBc.

The following figure illustrates how SFDR is measured.



# THD

The total harmonic distortion (THD) of a signal is the ratio of the sum of the powers of the first five harmonics above the measured fundamental frequency to the power of the fundamental frequency. THD is usually expressed in dB or dBc. Measurements for calculating the THD are made at the output of a device under specified conditions.

# SINAD

Signal-to-noise-and-distortion ratio (SINAD) is the ratio of the rms signal amplitude to the rms sum of all other spectral components, including the harmonics but excluding DC. SINAD is usually expressed in dB.

## Waveform Fundamentals ENOB

Effective number of bits (ENOB) is another way of specifying signal-tonoise and distortion ratio (<u>SINAD</u>). ENOB is calculated using the following formula:

 $ENOB = \frac{SINAD - 1.76}{6.02}$ 

Note Assumes the full scale of the DAC is utilized.

The ENOB value is the value of an ideal DAC that is equivalent to the DAC of the device.

## Waveform Fundamentals Filtering and Interpolation

All NI signal generators use a digital-to-analog converter (DAC) to generate the signals or waveforms that eventually appear at the output connector. These generated signals have a number of discrete voltage levels dependent on the number of bits in the DAC.

A digital waveform must be updated at least twice as fast as the bandwidth of the desired analog signal to be accurately generated (Shannon's Sampling Theorem). Even though the theoretical requirement for Sample clock,  $f_s$ , is twice that of the signal bandwidth,  $f_o$ , images are introduced in the output signal at  $|f_o \pm nf_s|$ , as shown in the following figure.



The images shown in the previous figure degrade the spectral purity of the signal, creating the need to filter these images out of the signal.

To create quality signals, all NI signal generators can lowpass filter the generated signal. A lowpass filter can smooth the raw DAC output. The filter removes high-frequency aliased components that are introduced through the digital generation of the signal. You can implement the lowpass filter through both analog and digital filters.

Designing an analog filter that rejects the images and yet gets maximum output bandwidth (0 to  $0.43f_s$ ) is difficult and is represented by the curve Analog Filter 1 in the following figure. Analog Filter 2 represents a more practical filter. This filter is not as aggressive as Analog Filter 1. Analog Filter 2 does not filter out the images near  $f_s$ , but it does reject all the others. Analog filters have trade-offs between the roll-off of the

attenuation after the 3 dB point and the flatness of the attenuation before the 3 dB point.

Another aspect of the analog filter is group delay—the amount of time needed for a signal having finite time duration, such as a pulse, to pass through the analog filter. Ideally, in an analog filter with linear group delay, all frequencies present in the signal should have the same time delay so that the signal is not distorted.

The third filter, Analog Filter 3, has a much higher 3 dB point than the first two analog filters. Because of the higher 3 dB point, the filter is very nearly flat in the passband (0 to  $0.43f_s$ ). Analog Filter 3 does not filter the images produced at  $f_s$  and  $2f_s$  at all, but this shortcoming can be alleviated with a digital interpolation filter.



To ease the requirements of the analog filter and to get more output bandwidth, NI signal generators use a halfband digital filter to interpolate one, three, or seven samples between every two waveform samples at two times, four times, and eight times the sample frequency,  $f_s$ . Also, the DAC operates at an effective sampling rate that is two times ( $2f_s$ ), four times ( $4f_s$ ) and eight times ( $8f_s$ ) the sample frequency—specifically, the rate at which the data is clocked from the memory into the DAC.

In the following figure, the two times interpolating filter is used and the effective sample rate of the DAC is  $2f_s$ . The images at  $f_s \pm f_o$  are no longer an issue, and the images are now at  $|2f_s \pm f_o|$ .



Now, Analog Filter 2 can easily filter out all the images due to the digital generation of the signal. This behavior is seen in the frequency domain representation in the previous figure and in the time domain representation in the following figure.



Note The allowable range of interpolation factors is dependent on the NI signal generator being used.

Using two times interpolation filtering with a DAC effective sample rate of  $2f_s$  eliminates images well and generates a good signal. However, increasing the interpolation filter to 4 further improves the output signal.

The following figure shows a signal image with four times interpolation, and the effective DAC sample rate at  $4f_s$ . The images are shifted up to  $4f_s$ , and well above the cutoff frequency of Analog Filter 3. This configuration eliminates the spectral images and has a filter that is maximally flat within the passband. This configuration approaches an ideal design in digitally generating spectrally pure waveforms.



To generate the most spectrally pure signals using the digital filter, you should use the highest interpolation factor that you can.

## Devices

Expand this topic for device-specific information about your NI signal generator.

## NI 5401/5404/5411/5431 **Features Supported**

The following table shows the features supported by the NI 5401/5404/5411/5431 signal generators.

### Note If your device is not listed here, refer to NI 5402/5406/5412/5421/5422/5441/5442 Features Supported

	NI 5401	NI 5404	NI 5411
<b>Basic Operation</b>	n	1	1
Output Modes	Standard Function, Frequency List	Standard Function (sine or square)	Standard Func Frequency L Arbitrary Wave Arbitrary Sequ
Standard Funct	ion Output		
Waveform	Sine, Square, Triangle, Ramp Up, Ramp Down, DC, Noise, User-Defined	Sine and Square (both are produced)	Sine, Square, Triangle, Ramp Up, Ramp Dow DC, DC, Noise, User-Define
Minimum Frequency	9.313 mHz	1 μHz	9.313 mHz
Maximum Frequency <mark>5</mark>	Sine: 16 MHz Other: 1 MHz	105 MHz	Sine: 16 MF Other: 1 MF
SYNC Duty Cycle	20% to 80%	—	20% to 80%
User-Defined Waveform Size	16,384 samples	16,384 samples	16,384 samp

## Frequency List Output

Frequency List	Output		
Maximum Number of Lists <u>*</u>	16		16
Maximum List Length <u>*</u>	512	—	512
Maximum Step Duration [±]	3.35544 s	—	3.35544 s
Minimum List Length <u>*</u>	1	—	1
Minimum Step Duration <mark>*</mark>	1 ms	—	1 ms
Step Duration Quantum [±]	200 ns	_	200 ns
Arbitrary Wave	form Output		<u> </u>
Write Quantum		_	64 samples or 32 compl samples
Waveform Quantum≛		—	8 samples
Minimum Waveform Size <u>*</u>		_	256 sample
Maximum Waveform Size <u>*1</u>		_	2 M or 8 M samp
Maximum Number of Waveforms*		_	5,000
Onboard Signal Processing		—	—
Arbitrary Seque	ence Output		
Minimum Sequence			1

Length [*]			
Maximum Sequence Length <u>*</u>		_	292
Maximum Loop Count <u>*</u>		_	65,535
Maximum Number of Sequences [*]		_	16
Onboard Signal Processing		_	—
<b>Output Charact</b>	eristics		
Output Voltage (at load equal to source impedance)	up to ±5 V	sine: 1 V _{pk-pk} to 2 V _{pk-pk} square: 5 V, 3.3 V, or 1.8 V	up to ±5 V
Offset (at maximum gain)	±2.5 V	—	±2.5 V
Output Impedance	50 Ω, 75 Ω	50 Ω	50 Ω, 75 Ω
Analog Path			
Analog Filter Option	Yes	_	Yes
Filter Correction Frequency Option	Yes	_	Yes
Digital Filter Option	Yes	_	Yes
Digital Filter Interpolation Factor	2 (fixed when filter is enabled)	_	2 (fixed when filt enabled)
DIGITAL DATA			Yes

& CONTROL CONNECTOR (DDC) or Digital Pattern			
Triggering and	Synchronization		
Trigger Modes (Frequency List and Arbitrary Waveform Generation Modes)	Single, Continuous, Stepped, Burst		Single, Continuous Stepped, Burst
Trigger Sources	Immediate, External, Software, RTSI_<05>, RTSI_6 (PCI only), PXI_STAR (PXI only)	Immediate, PFI 0 (External), Software, RTSI_<07>, PXI_STAR	Immediate External, Software, RTSI_<05: RTSI_6 (PCI o PXI_STAR (PXI
Multiple Device Synchronization	Limited ²	Standard Function Mode	Arbitrary Wave Generation a Sequence mo
Events		•	
Ready for Start			
Started	_	—	—
Done			—
Marker			Yes
Data Marker			
Clocking			
Sample Rate (Update Rate) before filtering and interpolation	40 MS/s	300 MS/s	Up to 40 MS
Reference Clock Source	Internal (none), External,	Internal (none),	Internal (non External,

	PXI 10 MHz clock (PXI only) or RTSI clock (PCI only)	External (REF IN), RTSI_<06>, RTSI clock, PXI 10 MHz clock	PXI 10 MHz cloc only) <i>or</i> RTSI clock (PC
Reference Clock Frequency	1 MHz <i>or</i> 5 to 20 · 1 MHz	3 to 20 · 1 MHz	1 MHz <i>or</i> 5 to 20 · 1 M
Clock Mode (Arbitrary Waveform Generation Mode)			Divide-Dow High-Resolut (PXI only)
Sample Clock Source (Arbitrary Waveform Generation Mode)			Internal, External (PXI (
Calibration	ł		
Self-Calibration Functions	ni54xx_CalSelfCalibrate, ni54xx_CalRestore ExternalConstants		ni54xx_CalSelfCa ni54xx_CalRes ExternalConsta
Calibration Utility Functions ³	ni54xx_ functions	ni54xx_ functions	ni54xx_ functi
External Calibration Functions ⁴	ni54xx_CalStart and associated functions	ni54xx_CalStart and associated functions	ni54xx_CalStart associated func

*You can get the value of this characteristic by calling a query function or by reading an attribute. NI recommends that your programs query or read the characteristic rather than depend on a certain value. ¹Varies with the device model or the amount of memory on the device. Memory use is a function of the number and size of waveforms and (in Arbitrary Sequence mode) the number and length of sequences. Typically, waveforms use most of the memory, but if you have a very large number of sequences, the available waveform memory is reduced.

²You can synchronize the NI 5401/5411/5431 in Standard Function mode as long as it is unnecessary to change the phase between devices while generating.

³NI 5401/5404/5411/5431 calibration utility functions include:

ni54xx_CalFetchDate

ni54xx_CalFetchCount

ni54xx_CalFetchMiscInfo

ni54xx_CalStoreMiscInfo

ni54xx_CalChangePassword

⁴External calibration functions and steps vary from device to device. For more information about calibrating your device, refer to the calibration procedure for your device:

NI 54XX Calibration Procedure (NI 5401/5411/5431)

NI PXI-5404 Calibration Procedure

⁵Refer to the <u>device specifications</u> for conditions.

## NI 5402/5406/5412/5421/5422/5441/5442 **Features Supported**

The following table shows the features supported by NI signal generators based on the <u>SMC</u> technology.



### Note If your device is not listed here, refer to NI 5401/5404/5411/5431 Features Supported

	NI 5402	NI 5406	NI 5412
Basic Operation	n		
Output Modes	Standard Function, Frequency List	Standard Function, Frequency List	Standard Function, Arbitrary Waveform, Arbitrary Sequence
Standard Funct	tion Output		
Waveform	Sine, Square, Triangle, Ramp Up, Ramp Down, DC, Noise, User-Defined	Sine, Square, Triangle, Ramp Up, Ramp Down, DC, Noise, User-Defined	Sine, Square, Triangle, Ramp Up, Ramp Down, DC, Noise, User-Defined
Minimum Frequency	0 Hz	0 Hz	<1 mHz ⁵
Maximum Frequency <del>4</del>	Sine: 20 MHz Square: 20 MHz User-Defined: 20 MHz Other: 1 MHz	Sine: 40 MHz Square: 40 MHz User-Defined: 40 MHz Other: 5 MHz	Sine: 20 MHz Square: 5 MHz Other: 1 MHz
1			I

SYNC Duty Cycle	20% to 80% for square	20% to 80% for square	
Lloor Dofined	50% for all other	50% for all other	1
Waveform Size	16,384 samples	16,384 samples	<u>Variable</u> [±]
<b>Frequency List</b>	Output		
Maximum Number of Lists <u>*</u>	9,999 lists	9,999 lists	
Maximum List Length <u>*</u>	58,253 s	58,253 s	
Maximum Step Duration <mark>*</mark>	21 s	21 s	
Minimum List Length <u>*</u>	1 s	1 s	
Minimum Step Duration <u>*</u>	1 ms	1 ms	
Step Duration Quantum <mark>*</mark>	80 ns	80 ns	
Arbitrary Wave	form Output		
Write Quantum	64 samples or 32 complex samples	64 samples or 32 complex samples	64 samples or 32 comple samples
Waveform Quantum <u>*</u>			4 samples
Minimum Waveform Size <u>*</u>	—		4 samples
Maximum Waveform Size <u>*1</u>			4 M, 16 M, 128 M sampl
Maximum Number of	—	—	2,097,151

Waveforms*			
Streaming			
Onboard Signal Processing	—		_
<b>Arbitrary Sequer</b>	nce Output		_
Minimum Sequence Length <u>*</u>			1
Maximum Sequence Length <u>*</u>	—		16,777,205
Maximum Loop Count <u>*</u>			16,777,215
Maximum Number of Sequences <u>*</u>	—		2,097,151
Streaming			
Onboard Signal Processing	—		_
Script Output			
Maximum Number of Script Triggers	—		_
Maximum Number of Markers	—		
Streaming			
<b>Output Characte</b>	ristics		
Output Voltage (at load equal to source impedance)	up to ±5 V	up to ±5 V	up to ±6 V
Offset	±5 V _{nk}	±5 V _{nk}	±3 V

(at maximum gain)				
Output Impedance	50 Ω, 75 Ω	50 Ω, 75 Ω	50 Ω, 75 Ω	
Analog Path	Main, Fixed Low-Gain, Fixed High-Gain	Main, Fixed Low-Gain, Fixed High-Gain	Main, Fixed Low-Gain, Fixed High-Gain	
Analog Filter Option	Yes	Yes	No	
Flatness Correction for Sine Waveforms	Yes	Yes		
Digital Filter Option	Yes	Yes	Yes	
Digital Filter Interpolation Factor	2 or 4 (automatic for Standard Function and Frequency List modes)	2 or 4 (automatic for Standard Function and Frequency List modes)	2, 4, or 8 (maximum of 400 MS/s) <i>or</i> automatic	
DIGITAL DATA & CONTROL CONNECTOR (DDC) or Digital Pattern				
Triggering and	Synchronization	•	•	
Trigger Modes (Frequency List and Arbitrary Waveform Generation Modes)	Single, Continuous, Stepped, Burst	Single, Continuous, Stepped, Burst	Single, Continuous, Stepped, Burst	
Trigger Sources	Immediate,	Immediate,	Immediate,	

	External, Software, RTSI_<07>, PXI_STAR PFI <01>	External, Software, RTSI_<07>, PXI_STAR PFI <01>	External, Software, RTSI_<07>, PXI_STAR PFI <01>
Multiple Device Synchronization	Using <u>NI-TClk</u>	Using <u>NI-TClk</u>	Using <u>NI-TClk</u> except for Standard Function mode
Events			
Ready for Start	Yes	Yes	Yes
Started	Yes	Yes	Yes
Done	Yes	Yes	Yes
Marker	—	—	Yes
Data Marker			
Clocking			
Sample Rate (Update Rate) before filtering and interpolation	100 MS/s	100 MS/s	Internal Sample clock: 10 S/s to 100 MS/s External Sample clock: 10 S/s to 105 MS/s
Reference Clock Source	Internal (none), External (CLK IN), PXI 10 MHz clock (PXI only), RTSI_7 (RTSI clock; PCI only), Onboard (PCI only)	Internal (none), External (CLK IN), PXI 10 MHz clock (PXI only), RTSI_7 (RTSI clock; PCI only), Onboard (PCI only)	Internal (none), External (CLK IN), PXI 10 MHz clock (PXI only), RTSI_7 (RTSI clock; PCI only), Onboard (PCI only)
Reference Clock Frequency	5 MHz to 20 MHz in 1 MHz steps	5 MHz to 20 MHz in 1 MHz steps	5 MHz to 20 MHz in 1 MHz steps
Clock Mode	_	_	Divide-Down,

(Arbitrary Waveform Generation Mode)			High-Resolution, Automatic
Sample Clock Source (Arbitrary Waveform Generation Mode)			Internal, External (CLK IN), PXI_STAR (PXI only), RTSI_<07>
Calibration			
Self-Calibration Functions	niFgen_SelfCal,	niFgen_SelfCal,	niFgen_SelfCal,
	niFgen_RestoreLast ExtCalConstants	niFgen_RestoreLast ExtCalConstants	niFgen_RestoreLast ExtCalConstants
Calibration Utility Functions ²	niFgen_ functions	niFgen_ functions	niFgen_ functions
External Calibration Functions ³	niFgen_InitExtCal and associated functions	niFgen_InitExtCal and associated functions	niFgen_InitExtCal and associated functions

*You can get the value of this characteristic by calling a query function or by reading an attribute. NI recommends that your programs query or read the characteristic rather than depend on a certain value.

¹Varies with the device model or the amount of memory on the device. Memory use is a function of the number and size of waveforms and (in Arbitrary Sequence mode) the number and length of sequences. Typically, waveforms use most of the memory, but if you have a very large number of sequences, the available waveform memory is reduced.

²Calibration utility functions include:

niFgen_GetSelfCalSupported

niFgen_GetSelfCalLastDateAndTime

niFgen_GetExtCalLastDateAndTime

niFgen_GetSelfCalLastTemp

niFgen_GetExtCalLastTemp

niFgen_GetExtCalRecommendedInterval

niFgen_ChangeExtCalPassword

niFgen_SetCalUserDefinedInfo

niFgen_GetCalUserDefinedInfo

niFgen_GetCalUserDefinedInfoMaxSize

niFgen_ReadCurrentTemperature

³External calibration functions and steps vary from device to device. For more information about calibrating your device, refer to the calibration procedure for your device:

NI 5402/5406 Calibration Procedure

NI 5412 Calibration Procedure

NI 5421/5441 Calibration Procedure

NI 5422 Calibration Procedure

⁴Refer to the <u>device specifications</u> for conditions.

⁵The minimum frequency available on these devices depends on the memory size of the device, as well as the value of the <u>NIFGEN_ATTR_FUNC_MAX_BUFFER_SIZE</u> attribute.

### NI PCI/PXI-5401 Overview

The NI 5401 is a 16 MHz function generator with the following features:

- One 12-bit resolution output channel
- Up to 16 MHz sine and transistor-transistor logic (TTL) waveform
  output
- Up to 1 MHz square, triangle, ramp up, and ramp down (DC and noise)
- Software-selectable output impedances of 50  $\Omega$  and 75  $\Omega$
- Output attenuation levels from 0 to 73 dB
- Phase-locked loop (PLL) synchronization to external clocks
- Sampling rate of 40 MS/s
- Digital and analog filters
- The Function Generation mode is implemented with 32-bit direct digital synthesis (DDS)
- External trigger input
- Real-Time System Integration (RTSI) and PXI triggers

All NI 5401 signal generators follow industry-standard Plug and Play specifications on both buses and offer seamless integration with compliant systems.

The <u>NI PXI/PCI-5401 Specifications</u> are included with the device and are also available at <u>ni.com/manuals</u>.

## NI PXI-5401 Front Panel Connectors

The following figure shows the front panels for the NI PXI-5401. Both the NI PXI-5401 and the NI PCI-5401 front panels contain three types of connectors: BNC, SMB, and 50-pin very high-density SCSI (VHDSCSI). The main waveform generates through the connector labeled ARB OUT on the PXI version ARB and on the PCI version.



### NI PXI/PCI-5401 ARB Connector

The ARB (PCI) or ARB OUT (PXI) connector provides the waveform output. The maximum output levels on this connector depend on the type of load termination. If the output of the NI PXI/PCI-5401 terminates into a 50  $\Omega$  load, the output levels are ±5 V, as shown in the following figure.



If the output of the NI 5401 terminates into a high-impedance load (HiZ), the output levels are  $\pm 10$  V. If the output terminates into any other load, the levels are as follows:

 $V_{out} = \pm [R_L / (R_L + R_O)] \times 10 \text{ V}$ 

where

Vout is the maximum output voltage level

 $R_1$  is the load impedance in ohms

 $R_O$  is the output impedance on the NI 5401

By default,  $R_O = 50 \Omega$ , but you can use the software to set it to 75  $\Omega$ .



Note Software sets the voltage output levels based on a 50  $\Omega$  load termination.

### NI PXI/PCI-5401 PLL Ref Connector

The PLL Ref connector is a <u>phase-locked loop (PLL)</u> input connector that can accept a Reference clock from an external source and frequency lock the NI PXI/PCI-5401 internal clock to the external clock. The Reference clock should not deviate more than ±100 ppm from its nominal frequency. This clock does not require the minimum amplitude levels of 1  $V_{pk-pk}$ . You can lock Reference clock frequencies of 1 MHz and 5– 20 MHz in 1 MHz steps.



**Note** You can frequency lock the NI PCI-5401 to other NI devices over the RTSI bus using the 20 MHz RTSI clock signal. You can frequency lock the NI PXI-5401 to other NI devices using the 10 MHz backplane clock.

If a external Reference clock is not available, the NI 5401 automatically tunes the internal clock to the highest accuracy possible.

### NI PCI-5401 Pattern Out Connector

Use the pattern out connector on the NI PCI-5401 to supply the external trigger input to the device.

### **Connector Pin Assignments**

The following figure shows the NI PCI-5401 50-pin VHDCI female connector.

		~	~	
	/	_		
DGND	50	25	1	EXT TRIG
NC	49	24		NC
DGND	48	23		NC
NC	47	22		NC
DGND	46	21		NC
NC	45	20		NC
DGND	44	19		NC
RELL	43	18		RELL
DGND	42	17		REU
RELL	41	16		RELL
DGND	40	15		RELL
RELL	39	14		RELL
DGND	38	13		REU
REU	37	12		REU
DGND	36	11		REU
RFU	35	10		RFU
DGND	34	9		RFU
RFU	33	8		RFU
DGND	32	7		RFU
RFU	31	6		RFU
DGND	30	5		RFU
RFU	29	4	1	RFU
DGND	28	3	1	RFU
RFU	27	2	1	RFU
DGND	26	1		RFU
			8	
		~		
			~	

### **Signal Descriptions**

The following table shows the pin names and signal descriptions used on the NI 5401 digital output connector.

Signal Name	Туре	Description
DGND	_	Digital ground.
EXT_TRIG	Input	External trigger–The external trigger input signal is a TTL-level signal that you can use to start or step through a waveform generation.
NC	_	Not connected.
RFU	_	Reserved for future use. Do not connect signals to this pin.
### SHC50-68 50-Pin Cable Connector

You can use an optional SHC50-68 50-pin to 68-pin cable for external trigger input. The cable connects to the digital connector on the NI PCI-5401. The following figure shows the 68-pin female connector pin assignments on the SHC50-68 cable.

	$\sim$			
			~	
RFU	1	35	۱Ì	DGND
RFU	2	36		DGND
RFU	3	37		DGND
RFU	4	38		DGND
RFU	5	39		DGND
RFU	6	40		DGND
RFU	7	41		DGND
RFU	8	42		DGND
RFU	9	43		DGND
RFU	10	44		DGND
RFU	11	45		DGND
RFU	12	46		DGND
RFU	13	47		DGND
RFU	14	48		DGND
RFU	15	49		DGND
RFU	16	50		DGND
RFU	17	51		DGND
RFU	18	52		DGND
RFU	19	53		DGND
RFU	20	54		DGND
RFU	21	55		DGND
RFU	22	56		DGND
RFU	23	57		DGND
RFU	24	58		RFU
NC	25	59		DGND
NC	26	60		DGND
NC	27	61		DGND
NC	28	62		DGND
NC	29	63		DGND
NC	30	64		DGND
NC	31	65		DGND
NC	32	66		DGND
NC	33	67		DGND
TRIG	34	68	ļ	DGND
			Ϊ	

EXT_TR

### NI PXI/PXI-5401 SYNC Connector

The SYNC output is a TTL version of the sine waveform generated at the output. The SYNC output has a very high-frequency resolution, with a software-programmable clock source for many applications. You can also dynamically vary the duty cycle of the SYNC output between 20% to 80% by software control. The SYNC output derives from a comparator connected to the analog waveform and provides a meaningful waveform only when you generate a sine wave on the ARB output. The following figure shows the timing relationship between the SYNC and analog output waveform.



 $t_p$  is the time period of the sine wave generating and  $t_w$  is the pulse width of the SYNC output. The duty cycle is  $(t_w/t_p) \times 100\%$ .

# NI PXI/PCI-5401/5411/5431 LOCK and ACCESS LEDs

The NI 5401/5411/5431 signal generators have two LEDs: LOCK and ACCESS.

### LOCK LED

The LOCK LED indicates basic hardware status.

Color	Indications
Off	The device phase-locked loop is currently not locked to a Reference clock source. This status is normal if the device has not been programmed to phase lock to a Reference clock source. This is an indication of a problem if the device has not been programmed to phase lock to a Reference clock source.
Amber	The device phase-locked loop is locked to the selected Reference clock source.



Note For more information, refer to Phase-Locked Loops and Module Synchronization.

### ACCESS LED

The ACCESS LED indicates the device state.

Color	Indications
Green	Indicates that the device is powered.
Yellow	Indicates that the computer is currently accessing the device.

# NI PXI/PCI-5401 Power-Up and Reset Conditions

When you power up the computer, the NI PXI/PCI-5401 is in the following state:

- The output is disabled and set to 0 V.
- The trigger mode is Continuous.
- The trigger source is automatic (the software provides the triggers).
- The digital filter is enabled.
- Output attenuation remains unchanged from its previous setting.
- The analog filter remains unchanged from its previous setting.
- Output impedance remains unchanged from its previous setting.

When you reset the device using NI-FGEN or another API, the NI 5401 is in the same state as shown at power-up with the following differences:

- Output attenuation is set to 0 dB.
- The analog filter is enabled.
- Output impedance is set to 50  $\boldsymbol{\Omega}$
- The PLL Reference source is set to internal tuning.
- The SYNC duty cycle is set to 50%.

# NI 5401 Theory of Operation

Expand this topic for information about the NI 5401 theory of operation.

# NI PXI/PCI-5401 Block Diagram

The following figure shows the block diagram for the NI PXI/PCI-5401.



# NI PXI/PCI-5401 Analog Output

Analog waveforms generate as follows:

- 1. The 12-bit digital waveform data is fed to a high-speed DAC.
- 2. A lowpass filter filters the DAC output.
- 3. This filtered signal is amplified before it goes to a 10 dB attenuator.
  - Note The DAC output can be fine-tuned for gain and offset. Since the offset is adjusted before the main attenuators and amplifier, the offset is referred to as pre-attenuation offset. The fine-tuning of gain and offset is performed by separate DACs.
- 4. The output from the 10 dB attenuator then goes to the main amplifier, which can provide up to  $\pm 5$  V levels into 50  $\Omega$ . An output relay can switch between ground level and the main amplifier.
- 5. The output of this relay goes to a series of passive attenuators.
- 6. The output of the attenuators goes through a selectable output impedance of 50  $\Omega$  or 75  $\Omega$  to the I/O connector.

The following figure shows the essential block diagram of analog waveform generation.



The following figure shows the timing relationships of the trigger input and waveform output.  $t_{d1}$  is the pulse width on the trigger signal.  $t_{d2}$  is the time delay from trigger to output on ARB output.



# NI PXI/PCI-5401/5411/5431 Output Attenuation

The following figure shows the output attenuator chain for the NI signal generators.



Resistor networks make up output attenuators and you can switch them in any combination. The maximum attenuation possible for NI PXI/PCI-5401/5411/5431 is 73 dB.



**Note** You can switch an additional 10 dB attenuator in the Analog path that is not shown in the previous figure.

By attenuating the output signal, you keep the dynamic range of the DAC; that is, you do not lose any bits from the digital representation of the signal because the attenuation is done after the DAC and not before it.

attenuation (in decibels) = -20 log¹⁰ ( $V_o / V_i$ )

where

 $V_o$  = desired voltage level for the output signal

V_i = input voltage level

Note For the NI PXI/PCI-5401/5411/5431,  $V_i = \pm 5$  V for a terminated load and  $\pm 10$  V for an unterminated load.

NI-FGEN calculates the value of the output attenuation chain, which you can control by changing the peak-to-peak amplitude parameter. Attenuation of 0 dB corresponds to an amplitude of 10 V_{pk-pk}. The maximum attenuation of 73 dB corresponds to an amplitude of 2.24 mV_{pk-pk}. Any amplitude less than 2.4 mV_{pk-pk} is coerced to this value.

# NI PXI/PCI-5401/5411/5431 Analog Filter Correction

NI signal generators can correct for slight deviations in the flatness of the frequency characteristic of the analog lowpass filter in its passband, as shown in the following figure.



A. Typical Analog Filter Characteristics

B. Corrected Filter Characteristics

C. Correction Applied

Curve A shows a typical lowpass filter curve. The response of the filter is stored in an onboard EEPROM in 1 MHz increments up to:

- 16 MHz for NI PXI/PCI-5401/5411
- 8 MHz for NI PXI/PCI-5431

Curve C is the correction applied to the frequency response. The resulting curve B is a flat response over the entire passband. If you want to generate a sine wave at a particular frequency with filter correction applied, you must specify that frequency through the software.



**Note** You can change the filter frequency correction at any time during waveform generation.

## NI PXI/PCI-5401/5411/5431 Output Enable

You can specify which feature to disconnect and connect different devices to the NI PXI/PCI-5401/5411/5431 during operation. However, even when the output enable relay is OFF, the waveform generation process continues internally on the NI PXI/PCI-5401/5411/5431.

You can change the output enable state at any time during waveform generation. When you change this setting, the bouncing of electromechanical relays in Function Generator/Frequency List mode on the NI PXI/PCI-5401/5411/5431 distorts the output signal for approximately 200 ms. In the Arbitrary Waveform/Arbitrary Sequence Waveform mode on the NI PXI/PCI-5401/5411/5431 the output signal is distorted for approximately 10 ms.

# NI PXI-5401/5411/5431 Direct Digital Synthesis Lookup Memory

The NI PXI-5401/5411/5431 uses a 32-bit, high-speed accumulator with a lookup memory and a 12-bit DAC for <u>direct digital synthesis</u>-based waveform generation.

You can use the lookup memory in Direct Digital Synthesis mode only. You cannot use the lookup memory in Arbitrary Waveform Generation mode. You can store one cycle of a repetitive waveform-a sine, triangular, square, or arbitrary wave-in the lookup memory. Then, you can change the frequency of that waveform by sending just one instruction. You can use Direct Digital Synthesis mode for very fine frequency resolution function generation. You can generate sine waves of up to 16 MHz for NI PXI-5401/5411 and 8 MHz for NI PXI-5431 with a frequency resolution of 10.0 mHz. Because this mode uses an accumulator, waveform generation loops back to the beginning of the lookup memory after passing through the end of the lookup memory.

The NI PXI-5401 uses a lookup waveform memory for storing the waveform and FIFO memory for storing the staging list, which contains multiple frequency list information. This FIFO is referred to as an instruction FIFO.

In Direct Digital Synthesis mode, each stage is made up of two instructions: the frequency and the time. The frequency instruction specifies the frequency of the waveform generation. The time instruction specifies the amount of time that the frequency generates.



**Note** You cannot specify the number of iterations for a waveform to generate in Direct Digital Synthesis mode.

# NI PXI/PCI-5401 Generating Waveforms

The NI 5401 generates waveforms using Function Generation mode, which is implemented with direct digital synthesis technology. Direct digital synthesis generates standard waveforms that are repetitive in nature, such as sine, TTL, square, and triangular waveforms. Function Generation mode using direct digital synthesis limits you to one waveform, and the waveform size must be exactly equal to 16,384 samples.

The following figure is a block diagram of the Data path for waveform generation.



The data for waveform generation comes from DDS lookup memory. This data is interpolated by a half-band digital filter then fed to a high-speed DAC. The data has a pipeline delay of 26 Sample clocks through this digital filter. Although the digital filter can be disabled through software, there is still a 26 Sample clock delay.

On the NI 5401, the high-speed DAC is always updated at 80 MHz, but the Sample clock for memory is 40 MHz.

# NI PXI/PCI-5401/5411/5431 Frequency Hopping and Sweeping

You can define a staging list for performing frequency hops and sweeps. The entire staging list uses the same waveform loaded into the lookup memory. All stages differ with the frequency generated.



Note The minimum time that a frequency should generate is 3 μs. Therefore, the maximum hop rate from frequency to frequency is 333 kHz.

The maximum number of stages that the instruction FIFO can store for Direct Digital Synthesis mode is 512.

# NI PXI/PCI-5401/5411/5431 Trigger Sources

Trigger sources are software selectable. By default, the device starts immediately unless a Start trigger is selected. You can also use an external trigger from a pin on the digital I/O connector, the RTSI bus trigger lines for PCI devices, or the PXI trigger bus TTL trigger lines on the backplane for PXI devices. The following figure shows the trigger sources for NI signal generators.



If you need to automatically trigger the waveform generation, use software to generate the triggers. You need a rising TTL edge for external triggering.

For external triggering, apply a rising-edge TTL signal to the EXT_TRIG input. This signal should remain de-asserted (logic low) until after the software has initialized the waveform generation.

# NI PXI/PCI-5401 RTSI/PXI Trigger Lines

The NI 5401 contains seven trigger lines and one RTSI clock line available over the RTSI bus to send and receive NI 5401-specific information to other devices that have RTSI connectors. The following figure shows the RTSI trigger lines and routing of NI 5401 signals to the RTSI switch.



The following figure shows the PXI trigger lines and routing of NI PXI-5401 signals to the RTSI switch.



The NI 5401 can receive a hardware trigger from another device as an RTSI trigger signal on any of the RTSI/PXI trigger lines.

You can also route signals as follows:

- Route the start trigger signal generated on the NI 5401 to other devices through any of the RTSI/PXI bus trigger lines.
- Route the SYNC output generated on the NI 5401 to other devices through any of the RTSI/PXI bus trigger lines. You can use this

signal to give other devices an accurate and fine frequency resolution clock.

#### • NI PCI-5401

For frequency locking to other devices as a master, the NI PCI-5401 sends an onboard 20 MHz signal to the RTSI Osc line as a device clock signal. For locking to other devices as a slave, the NI PCI-5401 receives the RTSI Osc line as an RTSI clock signal.

#### • NI PXI-5401

For frequency locking to other devices, the NI PXI-5401 receives the PXI backplane 10 MHz Osc as a Reference clock signal. All NI PXI-5401 signal generators use this common signal as the Reference clock for frequency locking.

# NI PXI/PCI-5401 Modes of Operation

The NI 5401 has three trigger modes: <u>Single</u>, <u>Continuous</u>, and <u>Stepped</u>.

## NI PXI/PCI-5401 Burst/Stepped Trigger Mode

Burst and Stepped trigger modes operate in the same fashion on the NI 5401.

After receiving a Start trigger, the waveform defined by the first stage generates until receiving another trigger. At the next trigger, the waveform of the previous stage completes before the waveform defined by the second stage generates. After the staging list completes, the waveform generation returns to the first stage and continues in a cyclic fashion.

You can use Burst trigger mode with both the Arbitrary Waveform Generation and Function Generation modes as follows:

The following figure shows a Burst trigger mode of operation for the NI 5401. Switching from stage to stage is phase-continuous. In this mode, the time instruction is not used. The trigger paces the waveform generation from one frequency to the other.



# NI PXI/PCI-5401/5411/5431 Single Trigger Mode

The waveform you define in the staging list generates only once by going through the entire staging list. Only one trigger is required to start the waveform generation.

You can use Single trigger mode with both the Arbitrary Waveform Generation and Function Generation modes.

• Arbitrary Waveform Generation mode—In the following figure, Arbitrary Waveform Generation mode uses stages 1, 2, and 3 to create a Single trigger mode of operation for Arb Generation Waveform mode. After the NI signal generator receives a trigger, the waveform generation starts at the first stage and continues through the last stage. The last stage generates repeatedly until you stop the waveform generation.





- **Note** You can settle to a predefined state by making the last stage emulate that state.
- **Function Generation mode**—In Function Generation mode, after the NI signal generator receives a trigger, the waveform generation starts at the first stage and continues through the last stage. The last stage generates repeatedly until you stop the waveform generation. The following figure shows a Single trigger mode of operation for Function Generation mode.



For example, assume that one cycle of a sine wave is stored in the Function Generation lookup memory. For stage 1,  $f_1$  specifies the sine frequency to be generated for time  $\Delta t_1$ ,  $f_2$  and  $\Delta t_2$  for stage 2, and so on. If the staging list contains four stages,  $f_4$  generates continuously until the waveform generation is stopped.

# NI PXI/PCI-5401/5411/5431 Continuous Trigger Mode

The waveform you define in the staging list generates infinitely by continually cycling through the staging list. After a trigger is received, the waveform generation starts at the first stage, continues through the last stage, and loops back to the start of the first stage, continuing until you stop the waveform generation. Only one trigger is required to start the waveform generation.

You can use Continuous trigger mode with both the Arbitrary Waveform Generation and Function Generation modes, as shown in the following figures.

#### **Continuous Trigger Mode for Arbitrary Waveform Generation Mode**

Start Trigger _____ Repeat until Stopped End of All Stages -End of All Stages -

### **Continuous Trigger Mode for Function Generation Mode**



# NI 5401/5411/5431 Phase-Locked Loops and Module Synchronization

The PLL consists of a voltage-controlled crystal oscillator (VCXO) with a tuning range of  $\pm 100$  ppm. This VCXO generates the main clock of 80 MHz.

The PLL can lock to a Reference clock source from the external connector, from a RTSI Osc line on the RTSI bus for NI PCI signal generators, or from a 10 MHz Osc line on the PXI backplane bus for NI PXI signal generators. You can also tune the PLL internally using a calibration DAC (CalDAC). NI performs this tuning during manufacturing.

The reference and VCXO clock are compared by a phase comparator running at 1 MHz. The loop filters the error signal and sends it to the control pin of the VCXO to complete the loop.

The following figure shows the block diagram for the NI signal generators PCI devices PLL circuit.



The following figure shows the block diagram for NI signal generators PXI devices PLL circuit.



You can frequency lock to an external Reference clock source of 1 MHz and from 5 MHz to 20 MHz in 1 MHz increments. The PLL can lock to a signal level of at least 1  $V_{pk-pk}$ .



Notes If two or more NI 5401 signal generators are locked to each other using the same Reference clock, they are frequency locked, but the phase relationship is indeterminate.

When generating a video waveform, do not phase lock the NI 5431 if the attribute or property for Video Waveform Type is used to set the internal frequency of the device.

The VCXO output of 80 MHz is further divided by four to send a 20 MHz device clock signal to the RTSI bus.

# NI PXI/PCI-5401 Specifications

For information about the NI PXI/PCI-5401 specifications, refer to the NI PXI/PCI-5401 Specifications. You can access these specifications by navigating to Start»All Programs»National Instruments»NI-FGEN»Documentation»Hardware Specifications, or you can visit ni.com/manuals.

### NI PXI/PCI-5401 Calibration

Before shipping you the NI PXI/PCI-5401, NI calibrated your device to ensure that all features are within specifications.

Calibration is a set of operations that compares the values indicated by a measuring instrument or measuring system to the corresponding values realized by external standards. The result of calibration can be used to determine the measurement error and can correct for it in the adjustment process.

The calibration process consists of verifying, adjusting, and reverifying a device. During verification, you compare the measured performance to an external standard of known measurement uncertainty to confirm that the product meets or exceeds specifications. During adjustment, you correct the measurement error of the device by adjusting the calibration constants and storing the new calibration constants in the EEPROM. The host computer reads the calibration constants and the software uses them to compensate for errors in the data and to present calibrated data to the user.

For more information about calibrating NI signal generators, refer to <u>ni.com/calibration</u>.

### NI PXI/PCI-5401 Accessories

National Instruments offers a variety of products to use with NI 5401 signal generators, including probes, cables, and other accessories, such as the following:

- Shielded and unshielded I/O connector blocks (SCB-68, TBX-68, CB-68)
- RTSI bus cables

The following table lists recommends part numbers for cables that you can use with the NI 5401.

Product	Cable Name	Part Number	Cable Description
NI PXI- 5401	SMB 110	763405-01	50 $\Omega$ SMB male to BNC male, 1 m coaxial cable
NI PXI- 5401	SMB 300	763388-01	50 $\Omega$ SMB male to alligator clip, 1 m cable

For more information about these products, visit <u>ni.com</u>.

# NI PXI/PCI-5401 Connector Blocks

The following table lists recommended part numbers for connector blocks that you can use with the NI 5401.

### National Instruments Connector Blocks

Product	Part Number	Description
SCB-68	776844- 01	Shielded I/O connector block for connection to cables with 68-pin connectors.
CA- 1000	777664- 01	Shielded enclosure for signal conditioning.
TBX-68	777141- 01	I/O Connector Block with DIN Rail Mounting.
CB- 68LP	777145- 01	Low-cost accessory with 68 screw terminals for easily connecting to 68-pin DAQ devices.
CB- 68LPR	777145- 02	Low-cost accessory with 68 screw terminals for easily connecting to 68-pin DAQ devices.

### NI 5402/5406 Overview

The NI 5402 is a 20 MHz, 14-bit function generator. The NI 5406 is a 40 MHz, 16-bit function generator. These devices have the following features:

- One 14-bit resolution output channel for the NI 5402; 16-bit resolution for the NI 5406
- Output amplitude up to 10  $V_{pk-pk}$  into a 50  $\Omega$  load
- Offset up to ±5  $V_{pk}$  including AC and DC components into 50  $\Omega$  impedance
- Up to 20 MHz sine output for the NI 5402; 40 MHz for the NI 5406
- Up to 20 MHz square output for the NI 5402; 40 MHz for the NI 5406
- Up to 1 MHz triangle, ramp-up, and ramp-down for the NI 5402; 5 MHz for the NI 5406
- Software-selectable output impedances (50  $\Omega$  or 75  $\Omega)$  and output attenuation levels from 0 dB to 51 dB
- PLL synchronization to external clocks or to PXI_CLK10
- NI-TClk support for multi-module synchronization. Refer to **Start»All Programs»National Instruments»NI-TClk** for more information.
- Sampling rate of 100 MS/s
- 32 MB of onboard frequency list memory
- Digital and analog filters
- Digital gain
- Two external trigger inputs
- PXI trigger/RTSI lines

All NI 5402/5406 devices follow industry-standard Plug and Play specifications for the PXI bus, and offer seamless integration with compliant systems.

# NI PXI-5402/5406 Front Panel

The following figure shows the NI PXI-5402/5406 front panel. This front panel has four BNC connectors.



The  $\underline{CH 0}$  connector is the analog output from which waveforms are generated.

The <u>REF IN</u> connector provides the device with an external Reference clock.

The <u>SYNC OUT/PFI0 and PFI 1</u> connectors are multi-directional connections for a number of different signals.
# NI 5402/5406 CH 0 Connector

The CH 0 connector provides the analog waveform output. The maximum output levels from this connector depend on the type of load termination. If the output of the module terminates into a 50  $\Omega$  load, the maximum output levels are ±5 V as shown in the following figure.



If the output of the module terminates into a high-impedance load (HiZ), the maximum output levels are  $\pm 10$  V. If the output terminates into any other load, the levels are as follows:

 $V_{out} = \pm [R_L / (R_L + R_O)] \times 10 \text{ V}$ 

**Note** For loads less than 50  $\Omega$ , load impedance compensation only supports combinations of a gain and load impedance that meet the previous V_{out} equation.

where

Vout is the maximum peak output voltage level

 $R_L$  is the load impedance in ohms

 $R_O$  is the output impedance of the module

By default,  $R_O = 50 \Omega$ , but you can set the output impedance to 75  $\Omega$  in NI-FGEN. Refer to the <u>niFgen Configure Output Impedance</u> VI or the <u>niFgen_ConfigureOutputImpedance</u> function for more information about configuring the output impedance.

You can set the amplitude of the generated output signal in terms of peak voltage by setting the gain value. NI-FGEN calculates and sets the correct amount of attenuation required for the desired gain value. Refer to the <u>Amplitude</u> property or the <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u> attribute for more information about configuring the output signal

amplitude.

## Load Impedance Compensation

The NI 5402/5406 has the ability to configure the output signal amplitude based on a user-configured load-impedance setting. This is desirable for using the NI 5402/5406 with loads that are between 0  $\Omega$  and a high impedance. Refer to the <u>module specifications</u> for information about the output impedance tolerance.

By default, NI-FGEN assumes that the load impedance is equal to the output impedance. If they do not match, you have the option to change the load impedance value that NI-FGEN uses in its load-impedance compensation algorithm. NI-FGEN takes the load impedance into account for setting the amplitude, and provides the amplitude specified in the configured gain setting, eliminating the need to use the voltage divider equation. NI-FGEN compensates to give the desired peak-to-peak voltage amplitude. Refer to the Load Impedance property or the <u>NIFGEN ATTR LOAD IMPEDANCE</u> attribute for more information about load impedance.

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**Note** The voltage output levels are set in the software and are based upon a 50  $\Omega$  load termination by default, or based on the load resistance as specified by the user.

For specifications about the waveform output signal, refer to the <u>module</u> <u>specifications</u>.

## NI 5402/5406 **REF IN Connector**

The REF IN front panel connector can accept an external Reference clock



**Caution** You must *not* change the Reference clock frequency while waveform generation is in progress. Only modify the frequency of the external clock before you start the waveform generation or after you stop the waveform generation.

## **External Reference Clock Input**

The REF IN connector is an input that can accept a Reference clock from an external source and phase lock the internal clock of the signal generator to this external Reference clock. Refer to the <u>module</u> <u>specifications</u> for the allowable Reference clock frequencies and signal characteristics.

The default value for the Reference clock source is Internal. Refer to the niFgen Configure Reference Clock VI or the niFgen_ConfigureReferenceClock function for more information about configuring the Reference clock source and frequency.



**Note** You can also phase lock the signal generator to other NI devices using the common PXI 10 MHz backplane clock for PXI or the RTSI 7 line for PCI. Refer to <u>PLL Reference Sources</u> for more information.

# NI 5402/5406 SYNC OUT/PFI 0 and PFI 1 Connectors

SYNC OUT/PFI 0 and PFI 1 are bidirectional connectors.

As an input, SYNC OUT/PFI 0 and PFI 1 terminals can accept a trigger from an external source that can start or step through waveform generation. As an output, the SYNC OUT/PFI 0 and PFI 1 lines can route a signal out from the following sources:

- SYNC OUT
- Out Start trigger
- PLL Reference Clock source
- Sample Clock Out (with *IK*, where K is an integer used to divide the Sample clock)

Refer to Exporting Signals for more information about routing signals. Refer to the module specifications for information about acceptable input signal characteristics to connect to the SYNC OUT/PFI 0 and PFI 1 lines, as well as the output signal characteristics.

Notes NI-FGEN routes SYNC OUT to the SYNC OUT/PFI 0 connector by default. To use the SYNC OUT/PFI 0 to import or export any other signal, you must unroute SYNC OUT by using the <u>niFgen Export Signal</u> VI or the <u>niFgen_ExportSignal</u> function. If you route a signal to SYNC OUT/PFI 0 without first unrouting SYNC OUT, NI-FGEN returns error -89137 (Hex 0xBFFA6B8E) noting that the specified route could not be satisfied.

SYNC OUT/PFI 0 driver circuitry has been optimized to have lower jitter than PFI 1 for exporting the SYNC OUT Sample clock or the PLL Reference clock source.

# NI 5402/5406/5412/5421/5422/5441/5442 Power-Up and Reset Conditions

The signal generator is in the following state from when the computer begins to power up until the operating system is fully booted and NI-FGEN is loaded.

- The CH 0 analog output connector is disabled and has 50  $\Omega$  or 75  $\Omega$  impedance to ground. This impedance is the same as its previous setting before the device was powered down. Also, the output voltage amplitude of this connector is 0 V.
- CLK IN and REF IN connectors have 50  $\Omega$  impedance to ground.
- PFI 0, SYNC OUT/PFI 0, and PFI 1 are tristated and have a 1  $k\Omega$  impedance to ground.
- In devices with a DDC connector, DIGITAL DATA & CONTROL output lines are disabled and floating; inputs have a 100  $\Omega$  differential termination.
- PXI trigger or RTSI lines are tristated and floating.

After the operating system is fully booted and NI-FGEN is loaded, or when you perform a hard reset to the device directly from MAX or using NI-FGEN, the signal generator is in the following state:

- CH 0 output is enabled.
- CH 0 output attenuation is set to 0 dB.
- Output impedance is set to  $50 \Omega$ .
- The Low-Gain Amplifier path is enabled in the Analog Output path.
- The analog filter is disabled.
- The digital filter of the NI 5402/5406/5412/5421/5441/5442 inside the DAC is disabled.
- CLK IN or REF IN is disabled and has a 50  $\Omega$  impedance to ground.
- PFI 0, SYNC OUT/PFI 0, and PFI 1 are tristated and have a 1  $k\Omega$  impedance to ground.
- On applicable devices, all output lines on the DIGITAL DATA & CONTROL Connector are disabled and floating; inputs have a 100  $\Omega$  differential termination.

- PXI trigger or RTSI lines are tristated and floating.
- The sample rate is set to the maximum rate, with the Sample clock source set to the internal Sample clock timebase.
- The Sample clock timebase is tuned by the internal reference control voltage.

# Thermal Shutdown

NI-FGEN supports thermal shutdown capability for NI 5402/5406/5412/5421/5422/5441/5442 signal generators. This capability allows the signal generator to detect when it has reached a dangerously high temperature and to then power down, preventing damage to the device.

Air circulation paths, fan settings, and space allowances are several factors that can influence device temperature. To prevent thermal shutdown, follow the guidelines described in the Maintain Forced-Air Cooling Note to Users document that shipped with your device. Refer to your <u>device specifications</u> to find the correct operating temperature range.

In the event that the signal generator powers down, you are notified with an error message in one of the following ways:

- NI-FGEN returns an error when you use any of the VIs or functions that program the hardware or check hardware status, for example, the <u>niFgen Commit</u> VI or the <u>niFgen_commit</u> function and the <u>niFgen Self Cal</u> VI or the <u>niFgen_SelfCal</u> function.
- Measurement & Automation Explorer (MAX) returns an error message if you run a self-test on your device after it exceeds the thermal shutdown temperature.

To re-enable your device after thermal shutdown, use one of the following methods:

• Power down the computer or chassis that contains the signal generator.

OR

 Call the <u>niFgen Reset Device</u> VI or the <u>niFgen_ResetDevice</u> function or perform a device reset in MAX. For more information about resetting a device in MAX, select Help»Help Topics»NI-DAQmx»MAX Help for NI-DAQmx within MAX.

Review the guidelines in the *Maintain Forced-Air Cooling Note to Users* document that shipped with the product and make any necessary adjustments to ensure that the digitizer is cooled effectively. The thermal shutdown error continues to be reported until the device is successfully reset.

# NI 5402/5406/5412/5421/5422/5441/5442 Theory of Operation

Expand this topic for information about the theory of operation of your signal generator.

# NI 5402/5406 Block Diagram

This topic contains information about the NI 5402/5406 top-level block diagram and descriptions of the individual blocks.



#### **Legend**



**Note** If it is installed in any slot other than Slot 2 of the PXI chassis, the NI 5402/5406 can receive a signal on the PXI_STAR line and can route a signal on the PXI_STAR line back to Slot 2 of the PXI chassis.

The following list describes the individual blocks:

- The *Onboard Memory* stores the <u>frequency list</u> instructions that you load into the device.
- *Clocking* allows you to phase lock the onboard Sample clock to a Reference clock.
- The *Standard Function Generation Engine* generates standard functions using <u>direct digital synthesis</u> (DDS) with a 16 k lookup table and 48-bit accumulator using the 100 MHz Sample clock.
- The Standard Function Generation Engine retrieves the frequency list instructions from the Onboard Memory.

- The output from the *Standard Function Generation Engine* is sent to the *DAC* after any digital gain is applied.
- For user-defined waveforms, the *DAC* also contains a selectable *Digital Filter*, which interpolates and filters the waveform data.
- The waveform data is sent from the *DAC* to the *Analog Output path* where the signal data is filtered and amplified.
- The *Routing Matrix* allows flexible routing of the PXI Trigger lines (RTSI) and the external PFI lines.

# NI 5402/5406/5412/5421/5422/5441/5442 Hardware State Diagram

The following diagram shows the hardware states of the signal generator.



The signal generator can be in one of six basic states during the course of operation.

**Idle**—The device is not generating a waveform. All session attributes can be programmed in the Idle state. In the Idle state, the attributes have not necessarily been applied to hardware, so the hardware configuration of the device may not match the session attribute values. The device remains configured as it was the last time a session was committed. Refer to <u>NI-FGEN Programming State Model</u> for information about when attributes are applied to the device. If the computer has just been powered on, reset, or the <u>niFgen Reset Device</u> VI or the <u>niFgen_ResetDevice</u> function has just been called, the device is in the default hardware state.

**Wait for Trigger**—After initiating generation, the device shifts to the Wait for Trigger state. If the trigger source is immediate, the device immediately shifts from this state and generates a Started event. If the

trigger sources are configured for a software trigger or for a hardware trigger from one of the available sources, the device remains in this state until the configured trigger occurs. When the device recognizes a trigger condition, the device immediately shifts out of this state and generates a Started event.

**First Data Appears**—This state is temporary and indicates that waveform data is just starting to appear at the CH 0 front panel connector.

**Generation**—In the Generation state, the device is generating a waveform as specified by the session attributes configured. Dynamic (or on-the-fly) properties and attributes, such as the <u>Amplitude</u>, <u>Arbitrary</u> <u>Waveform Gain</u>, and <u>Arbitrary Waveform Offset</u> properties, or the <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u>, <u>NIFGEN_ATTR_ARB_GAIN</u>, and the <u>NIFGEN_ATTR_ARB_OFFSET</u> attributes, are applied immediately to hardware. Started Event trigger is generated as the device recognizes triggers. Depending on the configured trigger mode, the device may stay in the Generation state until the generation is aborted.

Dynamic properties and attributes, such as amplitude, gain, and offset, can be applied to the device immediately if you set them while the session is in the Generation state. Refer to the <u>NI-FGEN LabVIEW</u> <u>Reference</u> or the <u>NI-FGEN C Function Reference</u> for information about the specific property or attribute that you want to set during generation.

**Done**—The device has completed the waveform generation as configured for this session. This state only occurs at the end of a generation state configured for the Single trigger mode. The device remains in this state until the you use NI-FGEN to abort the waveform generation and to return the device to the Idle state.

**Hardware Error**—An internal hardware error occurred, such as data underflow, the PLL became unlocked, the device shut down due to an over-temperature condition, and so on. The signal generator may still be generating and may be unpredictable at this point. When the driver software checks the status of the device, an error is returned.

# NI 5402/5406 Analog Output

The following figure shows the NI 5402/5406 Analog Output signal path.



### Legend

NI 5402/5406 Analog waveforms are generated as follows:

- The digital waveform data from the Standard Function Generation Engine is passed to a digital gain circuit and then high-speed DAC. This DAC also implements a portion of the output signal path attenuation with a range of 0 dB to 3 dB. Refer to the module <u>specifications</u> for the exact resolution. You can adjust the amount of attenuation by configuring the <u>Amplitude</u> property or the <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u> attribute. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting.
- 2. Following the DAC, the signal then passes through a switchable lowpass Analog Filter to remove <u>Aliased Images</u>. For Userdefined waveforms created in Standard Function mode or Frequency List mode, you can select whether to include the

Analog Filter in the Analog Output path using either the <u>niFgen</u> <u>Configure Analog Filter</u> VI or the <u>niFgen_EnableAnalogFilter</u> and <u>niFgen_DisableAnalogFilter</u> functions.

- 3. Either the Main path output or the Square Wave Output path is selected based on the desired waveform which then passes through the DC Offset Amplifier that adds the desired DC offset voltage. For User-defined waveform created in Standard Function mode or Frequency List mode, you can adjust the amount of DC offset added to the signal up to  $\pm 5 V_{pk}$  including AC and DC components into 50  $\Omega$  impedance. Refer to the DC Offset property, or the NIFGEN_ATTR_FUNC_DC_OFFSET attribute for more information.
- 4. The signal then passes through the Pre-Amp Attenuation section, a set of selectable solid-state attenuators that provide 0 dB to 12 dB of attenuation in 3 dB increments. You can adjust the amount of attenuation by adjusting the Amplitude property, or the NIFGEN_ATTR_FUNC_AMPLITUDE attribute. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting. Refer to the <u>Amplitude</u> property, or the <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u> attribute for more information.
- 5. Following the Pre-Amp Attenuation section, the signal can take one of two paths: the High-Gain or Low-Gain Amplifier path. NI-FGEN automatically selects the best amplifier path between the High-Gain and Low-Gain amplifiers by default based on the Amplitude property or the NIFGEN_ATTR_FUNC_AMPLITUDE attribute setting. Alternatively, you can set the signal path to remain constant regardless of the amplitude setting for applications requiring one path or the other. Refer to the Analog Path property or the NIFGEN_ATTR_ANALOG_PATH attribute for more information.
  - a. The High-Gain Amplifier path is used for waveform output voltages greater than  $\pm 1.0 \text{ V} (\pm 0.83 \text{ V} \text{ for sine waveforms})$  into 50  $\Omega$ . The amplifier has a fixed gain and is included in the signal path to enable the signal generator to provide the maximum V_{pk-pk}.
  - b. The Low-Gain Amplifier path is used for waveforms that

have all output voltages equal to or smaller than  $\pm 1.0$  V ( $\pm 0.83$  V for sine waveforms) into 50  $\Omega$ . The amplifier has a fixed gain.

- 6. The signal passes through the Post Amp Attenuation section, a set of two passive attenuators 12 dB and 24 dB. You can adjust the amount of attenuation by configuring the Amplitude property or the NIFGEN_ATTR_FUNC_AMPLITUDE attribute. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting.
- 7. The signal then passes through the Output Enable relay. When the Output Enable relay is disabled, ground is connected to the output through a 50  $\Omega$  or a 75  $\Omega$  resistor. Intentionally, Standard Function Generation continues while the output enable relay is disabled. When the relay is enabled, the analog waveform is seen at the CH 0 connector. You can enable or disable the output of the analog waveform generator. Refer to the <u>niFgen Output Enable</u> VI or the <u>niFgen ConfigureOutputEnabled</u> function for more information.
- The signal then passes through a 50 Ω/75 Ω selector to the CH 0 connector. You can configure the output impedance of the analog waveform generator, refer to the <u>niFgen Configure Output</u> <u>Impedance</u> VI or the <u>niFgen_ConfigureOutputImpedance</u> function.
- Note The NI 5402/5406 uses mechanical relays to switch between the optional sections in the Analog Out path. When you change a setting that results in a relay to switch, the bouncing of electromechanical relays on the NI 5402/5406 distorts the output signal for about 10 ms.

# NI 5402/5406 Waveform Amplitude Control

The NI 5402/5406 uses both amplifiers and attenuators to achieve needed amplitude settings.

## **Output Paths and Amplifiers**

The following figure shows two gain paths: the High-Gain Amplifier path and the Low-Gain Amplifier path.

The Low-Gain Amplifier path has a 2 V_{pk-pk} amplifier and is used for waveforms that have output voltages equal to or smaller than 2.00 V_{pk-pk} (1.67 V_{pk-pk} for sine waveforms) into matched load impedance. The High-Gain Amplifier path has a 10 V_{pk-pk} amplifier and is used for waveforms that have output voltages greater than 2.0 V_{pk-pk} (1.67 V_{pk-pk} for sine waveforms) into matched load impedance. The gains of the amplifiers are constant. Refer to the Amplitude property or the NIFGEN ATTR FUNC AMPLITUDE attribute for more information.

By default, NI-FGEN automatically selects the High-Gain and Low-Gain Amplifiers based on the amplitude setting. You can override NI-FGEN and configure the High-Gain or the Low-Gain Amplifier to remain in the Analog Output path regardless of amplitude by setting the <u>Analog Path</u> property or the <u>NIFGEN ATTR ANALOG PATH</u> attribute. Configuring the Low-Gain Amplifier path to remain constant regardless of the amplitude setting affects the maximum output value allowable for that particular amplitude setting. The maximum amplitude setting for an Analog Output path configured to Low-Gain Amplifier path is 2.0 (1.67 V_{pk-pk} for sine waveforms). The maximum allowable amplitude setting with NI-FGEN automatically selecting the Gain Amplifier path is 10.0 V with a high load impedance.

In addition, the DC Offset Amplifier for adding <u>DC offset</u> to the signal is in the High-Gain and Low-Gain Amplifier paths prior to the attenuators and amplifiers. The DC Offset Amplifier can be fine-tuned for adding offset to your signal. This fine-tuning of the main DC Offset Amplifier is performed by the Offset DAC.

### **Square Wave Path**

The NI 5402/5406 uses dedicated hardware to generate low-jitter square wave functions. A comparator is fed two signals: a sine tone from the main DAC (using the Digital Filter and the Analog Filter to obtain a 400 MS/s signal) and a DC signal using the Level DAC.

The output of the comparator is switched back into the Main path in order to obtain the desired amplitude and offset. The fine gain control of the signal is controlled through the Square Wave Gain DAC.

When the signal generator is configured to generate a square waveform, NI-FGEN automatically selects the Square Wave path. When the device is idle, it generates the low state of the square waveform.

When using the Square Wave path, the  $\underline{DC Offset}$  can be  $\pm 50\%$  of the current Amplitude.

The SYNC OUT is generated through the same comparator and is routed by default to the SYNC OUT/PFI 0 connector. You can unroute this route or change the output terminal of SYNC OUT using the <u>niFgen Export</u> <u>Signal</u> VI or the <u>niFgen_ExportSignal</u> function.

## NI 5402/5406 Attenuation

The Analog Output signal path has two passive attenuation sections. Pre-Amp Attenuation is prior to the High-Gain and Low-Gain Amplifier paths, and Post-Amp Attenuation is after the High-Gain and Low-Gain Amplifier paths. In addition, the main DAC provides 0 dB to 3 dB of signal attenuation. The amplitude control is implemented after the DAC. Attenuating the DAC output signal allows you to vary your signal amplitude and still maintain the dynamic range of the DAC. You do not lose any bits from the digital representation of the signal as does the method of controlling amplitude by using smaller data ranges of the DAC, sacrificing dynamic range.

For the Low-Gain Amplifier and the High-Gain Amplifier paths, maximum attenuation is 51 dB. NI-FGEN automatically determines the correct value of attenuation in dB, and configures the attenuation based on the set amplitude. The minimum amplitude setting for an Analog Output path configured to High-Gain Amplifier path with a 50  $\Omega$  load impedance is .01691 V. The minimum allowable amplitude setting with NI-FGEN automatically selecting the Low-Gain Amplifier path with a 50  $\Omega$  load impedance is .005635 V.

NI-FGEN calculates and sets the correct amount of attenuation required that corresponds to your NI-FGEN amplitude setting. The correct amount of attenuation is implemented in the Pre-Amp and Post-Amp Attenuation sections to best achieve the desired output signal amplitude. You can set the amount of amplitude with the <u>Amplitude</u> property or the <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u> attribute.

### **Pre-Amp Attenuation**

The Pre-Amp Attenuation section is before the Low-Gain and High-Gain amplifiers. The attenuators provide a range of attenuation from 0 dB to a maximum of 12 dB in steps of 3 dB. NI-FGEN automatically controls the value of attenuation set in the Pre-Amp Attenuation section depending on the set amplitude. You can read the value NI-FGEN has selected for Pre-Amp Attenuation using the Pre-Amplifier Attenuation property or the NIFGEN ATTR PRE AMPLIFIER ATTENUATION attribute.

Pre-Amp Attenuation improves the distortion of a signal because amplifiers provide lower distortion performance with smaller signals. However, attenuation lowers the amplitude of both the signal and the noise in a signal as the signal-to-noise ratio is unchanged upon attenuation. Amplifiers also have a fixed noise associated with them. The total noise at the amplifier output is obtained by taking the root of the sum of squares of the following factors:

- The input signal noise multiplied by the gain of the amplifier
- The amplifier noise

The total noise is dominated by the larger factor. If the signal is attenuated so that its noise when multiplied by gain at the amplifier input is smaller than the amplifier noise, then the output has a higher signal-tonoise ratio. This is a good reason to implement some of the signal generator overall attenuation as Post-Amp attenuation.

### **Post-Amp Attenuation**

The Post-Amp Attenuation section is after the High-Gain and Low-Gain Amplifiers. The attenuators provide a range of attenuation from 0 dB to a maximum of 36 dB in steps of 12 dB. NI-FGEN automatically controls the value of attenuation set in the Post-Amp Attenuation section dependent on the set amplitude. You can read the value NI-FGEN has selected for Post-Amp Attenuation using the Post-Amplifier Attenuation property or the NIFGEN_ATTR_POST_AMPLIFIER_ATTENUATION attribute.

### **DAC** Attenuation

The main DAC output can be fine-tuned for attenuation, which provides 0 dB to 3 dB of the Analog Output path signal attenuation. This finetuning of the main DAC attenuation is performed by the Gain DAC. You can adjust the Gain DAC using the <u>Gain DAC Value</u> property or the <u>NIFGEN_ATTR_GAIN_DAC_VALUE</u> attribute. The main DAC also provides the fine resolution for the attenuation settings.

The fine gain control of square wave signals is controlled through the Square Wave Gain DAC. You can adjust the Square Wave Gain DAC by setting the Gain DAC Value property or the NIFGEN_ATTR_GAIN_DAC_VALUE attribute.

## NI 5402/5406 DC Offset

The maximum DC Offset allowed on the signal generator depends on the output waveform being generated.

For square waveforms, the maximum offset that is allowed is 50% of the amplitude setting (50% of  $V_{pk-pk}$ ). The maximum offset is shown in the following figure.



For sine, triangle, ramp waveform or a user-defined waveform is generated, then any offset is allowed as long as the waveform stays within the +10 and -10 V amplitude limit of the board into high Z (+5 V and -5 V limit into 50  $\Omega$  load). A 2 V_{pk-pk} sine waveform is shown in the following figure with its maximum allowed offset setting.

+1 V 0 -1 V Waveform No Offset 2 V_{pk-pk} into High Z +10 V +8 V 2 V_{pk-pk} into High Z Maximum Positive Offset 3 (Offset = +9 V) 0 0 -8 V -10 V -Maximum Negative Offset (Offset = -9 V)

Note Using DC offset causes a reduction in DAC resolution and affects the Sync Out signal duty cycle for all waveforms except square waves. Refer to the <u>specifications</u> for more information.

# NI 5402/5406/5412/5421/5422/5441/5442 Digital Gain

Digital gain multiplies waveform data by a factor you specify in the <u>Digital</u> <u>Gain</u> property or the <u>NIFGEN_ATTR_DIGITAL_GAIN</u> attribute before converting the data to an analog signal in the DAC. Digital gain can be changed during generation without the glitches caused to relay switching that are common when changing analog gains. However, the output resolution of the DAC is a function of digital gain, so only analog gain makes full use of the resolution of the DAC.



**Note** When the NI 5402/5406 generates square waveforms, only a digital gain of 1.0 is supported.

# NI 5402/5406 Flatness Correction

The NI 5402/5406 uses flatness correction to ensure a consistent power level when generating sine waveforms at any frequency.

During external calibration, the frequency response of the Analog path in its different configurations is measured using the <u>niFgen Initialize</u> <u>Flatness Calibration</u> VI or the <u>niFgen InitializeFlatnessCalibration</u> function and the <u>niFgen Cal Adjust Flatness</u> VI or the <u>niFgen CalAdjustFlatness</u> function.

During generation, these measured values are used to compensate for any attenuation at the requested frequency. The compensation is applied by digitally multiplying the digital data going into the DAC by a correction factor.

# NI 5402/5406/5412/5421/5422/5441 Filtering Effects

The delay from trigger to analog output increases if the digital and/or analog filters in the Analog Output path are enabled. In the case of digital filtering, delay also increases with increase in interpolation. Enabling the <u>onboard signal processing block</u> can also introduce delay.



**Note** The digital filter for the signal generator is inside the main DAC shown in the Analog Output path.

Refer to <u>Digital Filter</u> for interpolation options. Refer to the <u>module</u> <u>specifications</u> for the delay from trigger to analog output based on different filtering options.

# NI 5402/5406/5421/5422/5441/5442 Analog Filter

The analog filter is a lowpass filter that is used to eliminate <u>aliased</u> images and artifacts due to the digital-to-analog conversion from the signal from the DAC. In general, use the analog filter for signals containing a large portion of sinusoidal content, such as AM and FM, sinc pulse, and sinusoidal chirp waveforms. The filter can be bypassed for signals that are better represented without filtering, such as square waves or waveforms containing many pulse characteristics. You can set the enabled state of the analog filter in the Analog Output path. Refer to the <u>niFgen Configure Analog Filter</u> VI or the <u>niFgen EnableAnalogFilter</u> and <u>niFgen_DisableAnalogFilter</u> functions for more information about setting the analog filter.



**Notes** NI recommends that the analog filter and digital filter always be enabled or disabled at the same time.

The analog filter is not available on the NI 5421/5422/5441/5442 when the Direct path is selected.

The delay from the time the device receives a Start trigger to the time a signal is generated at the analog output increases if the analog filter in the Analog Output path is enabled. Refer to the <u>device specifications</u> for information about the delay from the trigger to the analog output based on the configured filter settings.

### **Related Topic**

Filtering and Interpolation

# NI 5402/5406/5412/5421/5441 Digital Filter

The main DAC provides a digital filter internally. When digital filtering is enabled, the main DAC runs at a faster rate, referred to as the effective sample rate (ESR). The waveform data transfers to the main DAC at the configured Sample clock rate; the internal digital filter interpolates by a factor of 2x, 4x, or 8x; and the DAC generates the data at the ESR.

Effective sample rate is calculated with the following formula:

 $ESR = I_{fac} \times SR$ 

where

ESR = the Effective Sample Rate (MS/s)

 $I_{fac}$  = the interpolation factor

SR = configured Sample Clock Rate (MS/s)

The effective sample rate only applies when the digital filter is enabled. The maximum ESR is 400 MS/s. The effective sample rate is recommended to be as high as possible without exceeding 400 MS/s. The following table lists the allowed update and interpolation rates.



**Note** When the <u>onboard signal processing block</u> is enabled, you cannot set the <u>Sample Rate</u> property or the <u>NIFGEN_ATTR_ARB_SAMPLE_RATE</u> attribute. After you have configured the <u>IQ Rate</u>, you can read the sample rate.

Recommended Interpolation Settings		
Sample Clock Rate (MS/s)*	Interpolation	
12.5 to 105	2x	
10 to 100	4x	
10 to 50	8x	

*Note The NI 5402/5406 only supports a Sample clock rate of 100 MS/s.

Notes The digital filter is not available for use for Sample clock rates below 10 MS/s.

In Standard Function mode, the digital filter is enabled and disabled

by NI-FGEN except when generating user-defined waveforms.

The delay from the Start trigger to the analog output increases if the digital filter is enabled. The delay increases with an increase in the interpolation factor. Refer to the <u>module specifications</u> for information about the delay from the trigger to the analog output based on the configured filter settings.

In general, use the digital filter for signals containing large sinusoidal waveform content, such as AM and FM, sinc, and sinusoidal chirp waveforms. The filter can be disabled for signals that are better represented without filtering, such as square waves or waveforms containing many pulse characteristics. If you enable the digital filter without setting the interpolation factor, NI-FGEN automatically uses the highest interpolation factor possible in accordance with the above table. Refer to the Configure Digital Filter VI or the niFgen_EnableDigitalFilter and niFgen_DisableDigitalFilter functions for more information.

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**Note** It is recommended that the analog filter (if available) and digital filter are always enabled or disabled together.

### **Related Topics**

Filtering and Interpolation Aliased Images

# NI 5402/5406/5412/5421/5422/5441 Output Enable

You can switch off the analog output at the CH 0 connector by controlling the Output Enable relay, as shown in the following figure.



When the Output Enable relay is disabled, the output signal is connected to ground through a 50  $\Omega$  or 75  $\Omega$  resistance depending on the output impedance selected. The Output Enable relay is enabled for normal waveform generation, connecting the CH 0 SMB connector to Analog Output path. You can change the output enable state at any time during waveform generation and the generation continues on internally.

Refer to the <u>niFgen Output Enable</u> VI or the <u>niFgen_ConfigureOutputEnabled</u> function for more information about Output Enable.

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**Note** The signal generator uses mechanical relays to switch between the Output Enable states. When you change a setting that results in a relay to switch, the bouncing of electromechanical relays interrupts the output signal for up to 10 ms.

# NI 5402/5406 Output Impedance

The NI 5402/5406 Analog Output path is designed to have an output impedance of 50  $\Omega$  from the Output Enable relay looking back towards the Main DAC. There is a selectable 25  $\Omega$  resistance that can be switched into the Analog Output path between the Output Enable Relay and the CH 0 connector for applications requiring a 75  $\Omega$  impedance. Most applications use a load impedance of 50  $\Omega$ , but applications such as video testing, require 75  $\Omega$ . Refer to the following figure.

### **Legend**

If the load impedance is a high impedance (~1 M $\Omega$ ), you may see output levels up to twice the selected output value for a matched input/output impedance. These levels can be as high as 20 V_{pk-pk} for the High-Gain Amplifier path. Normally, the output levels increase as the load impedance increases. The NI 5402/5406 can compensate for different load impedance values. Refer to <u>CH 0 Connector</u> for more information.

You can select an output impedance of 50  $\Omega$  or 75  $\Omega$ . Refer to the <u>niFgen</u> <u>Configure Output Impedance</u> VI or the <u>niFgen_ConfigureOutputImpedance</u> function for more information.

**Note** The NI 5402/5406 uses mechanical relays to switch between the 50  $\Omega$ /75  $\Omega$  switch states. When you change a setting that results in a relay to switch, the bouncing of electromechanical relays on the NI 5402/5406 interrupts the output signal for up to 10 ms.

# NI 5402/5406 Clock Source and Frequency

The NI 5402/5406 has a sample clock rate of 100 MHz. You can use the REF IN connector or the PXI_CLK_10/RTSI 7 line as the source of the frequency reference for the onboard phase-locked loop. For PCI signal generators, you can also use the onboard Reference clock.



Note The onboard Reference clock is available only on PCI signal generators.

#### **Related Topics**

Phase-Locked Loop Reference Sources

**Exporting Clocks** 

# NI 5402/5406 Sample Clock

The signal generator provides a high-precision 100 MHz Voltage Controlled Crystal Oscillator (VCXO) clock source for the Sample clock timebase. The Sample clock timebase frequency is tuned by an Internal Calibration DAC Control Voltage. This clock is used to drive the DAC and all other waveform generation operations on the device. The Internal Calibration DAC, which is calibrated at the factory and which you can also calibrate, provides for the Sample clock timebase to maintain a high quality frequency source.

# NI 5402/5406 Phase-Locked Loop Reference Clock

A phase-locked loop (PLL) is a circuit that tunes the Sample clock timebase to phase–lock to an external Reference clock. The frequency stability and accuracy of the Sample clock timebase matches that of the Reference clock when the two phase–lock. Using the PLL on your device enables you to frequency-lock multiple devices in a single chassis, or devices in separate chassis.

Note Refer to the <u>module specifications</u> for information about the phase-locked loop reference frequencies available on your device.

The following figure shows the NI 5402/5406 Reference Clock Source path.



### Legend

To begin the PLL, the phase comparator compares the selected Reference clock to the 100 MHz clock of the Sample clock timebase. Next, a control voltage proportional to the phase difference between the two clocks is developed and used to tune the Sample clock timebase into alignment with the Reference clock. Finally, the Sample clock timebase output is routed back to the phase comparator, closing the loop.

Note When the <u>Reference Clock Source</u> property or the <u>NIFGEN_ATTR_REFERENCE_CLOCK_SOURCE</u> attribute is set to "None", the internal calibration DAC generates the calibration voltage and the PLL circuit is not used.

## **Reference Clock Sources**

The NI 5402/5406 is capable of phase–locking its Sample clock timebase to either an external signal on the REF IN front panel connector. PXI devices can also phase–lock to a 10 MHz Reference clock signal provided by the PXI bus (PXI_CLK10), while PCI devices can phase–lock to RTSI line 7 or to the onboard Reference clock.

The following table shows the valid NI-FGEN property or attribute values and combinations to configure the NI 5402/5406 clock settings for an external Reference clock.

Sample Clock Source	PLL Reference Clock Source
Internal VXCO(100 MHz)	"None" (default)
	"PXI_CLK10" (PXI), "RTSI7" (PCI)
	"RefIn"
	"OnboardRefClk" (PCI)

Refer to the <u>module specifications</u> for information about available REF IN signal levels.

Refer to the <u>niFgen Configure Reference Clock</u> VI or the <u>niFgen_ConfigureReferenceClock</u> function for more information about setting up the clock.
#### NI 5402/5406 Exporting Clocks

The NI 5402/5406 provides two resources for exporting your clocks and multiple destinations to route to.



The following table shows the available clock signals that can be routed to devices external to the NI 5402/5406 and the destination options.

Clock to be Exported	Destination Options
Sample Clock	SYNC OUT/PFI 0 and PFI 1 BNC connector
	PXI_Trig<06> (PXI), RTSI<06> (PCI)
Reference Clock	SYNC OUT/PFI 0 and PFI 1 BNC connector
	PXI_Trig<06> (PXI), RTSI<06> (PCI)
Onboard Reference Clock	RTSI7

#### Sample Clock

For synchronization purposes, the NI 5402/5406 allows you to export your Sample clock so that other devices can have the same timing as the NI 5402/5406. The Sample clock can be routed to the SYNC OUT/PFI 0 and PFI 1 front panel BNC connectors, PXI_Trig<0..6> lines on the PXI trigger bus, or the RTSI<0..6> (PCI) lines.

Additionally, the exported clock can be divided down by an integer value (no less than 2) before being exported to the SYNC OUT/PFI 0 and PFI 1 BNC connectors, PXI_Trig<0..6> lines, or the RTSI<0..6> (PCI) lines. Refer to the Exported Sample Clock Divisor property or the NIFGEN_ATTR_EXPORTED_SAMPLE_CLOCK_DIVISOR attribute for more information about configuring the Sample clock divisor.



**Note** For the maximum frequency that can be routed to the PXI trigger bus, or the RTSI<0..6> (PCI) lines, refer to the module <u>specifications</u>.

#### **Reference Clock**

For synchronization purposes, the NI 5402/5406 allows you to export your PLL Reference clock so that other devices can lock their clock sources to the same signal. Referring to the previous image, this clock is the actual clock that is configured for the NI 5402/5406 phase-locked loop circuit to use as a reference. You must have a Reference clock configured as a PLL Reference clock source for the signal to be available for exporting. The Reference clock can be routed to the SYNC OUT/PFI 0 and PFI 1 BNC connectors on the front panel, the PXI_Trig<0..6> lines on the PXI trigger bus, or the RTSI<0..6> (PCI) lines.



**Note** Although NI-FGEN allows values for Reference clock frequency on the NI 5402/5406 from 1 MHz to 20 MHz in 1 MHz increments, the NI 5402/5406 specifications are only valid with Reference clock frequencies from 5 MHz to 20 MHz.

#### **Onboard Reference Clock**

The onboard Reference clock is a dedicated 10 MHz clock for PCI modules only. The onboard Reference clock can only be exported to RTSI7, for other modules to use, and to reimport as the Reference clock. You can export the onboard Reference clock to other modules on RTSI7 and then reimport it so that all devices (including the master) can use the same Reference clock.

#### **Destination Options**

**SYNC OUT/PFI 0 and PFI 1**–The Sample clock and the Reference clock can be exported to the SYNC OUT/PFI 0 and PFI 1 BNC connectors on the front panel to synchronize external devices. You must configure the device to export the desired clock to the PFI BNC connectors.

Notes NI-FGEN routes SYNC OUT to the SYNC OUT/PFI 0 connector by default. To use the SYNC OUT/PFI 0 to import or export any other signal, you must unroute SYNC OUT by using the <u>niFgen Export Signal</u> VI or the <u>niFgen_ExportSignal</u> function. If you route a signal to SYNC OUT/PFI 0 without first unrouting SYNC OUT, NI-FGEN returns error -89137 (Hex 0xBFFA6B8E) noting that the specified route could not be satisfied.

SYNC OUT/PFI 0 driver circuitry has been optimized to have lower jitter than PFI 1 for exporting the SYNC OUT Sample clock or the PLL Reference clock source.

**PXI_Trig<0..6>**—The Sample clock and the Reference clock can be exported to the PXI_Trig lines or RTSI (PCI) lines. The PXI/PCI standard allows for devices to route signals to other devices in your PXI chassis to enhance device to device synchronization. Refer to the chassis documentation for specifications to ensure the reference signal is within tolerance. You must configure the device to export the desired clock to the PXI_Trig line or RTSI line. When exporting signals, PXI_Trig<0..6> is equivalent to RTSI_<0..6>

Refer to the <u>niFgen Export Signal</u> VI or the <u>niFgen_ExportSignal</u> function for more information about configuring the destinations for the desired clock signal.

## NI 5402/5406 Onboard Memory

The NI 5402/5406 can store the following in onboard memory:

- Up to 32 MB of frequency list instructions
- 65,536 samples for sine, square, and triangle waveforms
- 16,384 samples for all other waveforms

# **Signal Routing**

An NI signal generator is capable of sending and receiving signals through the front panel and the PXI or RTSI trigger bus. The front panel connectors provides connectivity for the output channel as well as for control lines for sending and receiving clocks, triggers, and events. You can use the PXI and RTSI trigger bus to send and receive events, triggers, and Sample and Reference clocks.

All signal routing operations can be characterized by a *source* and a *destination*. To determine the possible signal routes for your device, complete the following steps.

- 1. Launch MAX, either by navigating to **Start»All Programs»National Instruments»Measurement & Automation** or by double-click the **Measurement & Automation** icon on the desktop to open MAX.
- 2. Expand Devices and Interfaces. Expand NI-DAQmx Devices.
  - Note If you are using a remote RT target, expand **Remote Systems**, find and expand your target, and then expand **Devices and Interfaces**.
- 3. Select your device. The view to the right of the MAX configuration tree shows the attributes of your device.
- 4. Click the **Device Routes** tab below the attributes view. A table in the **Device Routes** view shows the possible sources and destinations for the signal generator. Sources are listed in the far left column, and the possible destinations span the top of the table. Each cell in the table is an index with the valid source and destination terminal for the device.

If a route is possible between a source and destination terminal, the intersecting cell is colored green or yellow. A green cell indicates the route can be made without consuming any important resource of your device. A yellow cell indicates that although the route is possible, something important must be consumed to create the route. Placing the cursor over a yellow square reveals the resource used in the **subsystem used** indicator.

5. Use the <u>niFgen Export Signal</u> VI or the <u>niFgen_ExportSignal</u> function to route the signals. For terminal name syntax, refer to

Syntax for Terminal Names.

**Tip** You can use the <u>niFgen Export Signal</u> VI or the <u>niFgen ExportSignal</u> function to route the same signal to multiple destinations.

## **Syntax for Terminal Names**

The syntax for terminal names is a unique identifier that refers to a physical terminal in your system. To guarantee the uniqueness of a terminal name across multiple devices, terminal names begin with a forward slash, followed by the name of the device as configured in MAX, such as Dev1. A forward slash and the name of the terminal follow the device identifier, such as PFI3. For example, the fully qualified terminal name for PFI3 on Dev1 is /Dev1/PFI3.

## **Waveform Generation**

NI signal generators can support one or more of the following output, or generation, modes:

- <u>Standard Function</u>
- <u>Arbitrary Waveform</u>
- <u>Arbitrary Sequence</u>
- <u>Script</u>
- Frequency List

To select an output mode, set the **Output Mode** parameter of the <u>niFgen</u> <u>Configure Output Mode</u> VI or the <u>niFgen_ConfigureOutputMode</u> function.

Refer to <u>Features Supported</u> to determine the output modes supported by your device.

## **Frequency List Mode**

In Frequency List mode, the device generates a standard function using a list of frequencies you define. A frequency list is composed of steps, each one with a frequency/duration pair. Frequency lists are commonly used for frequency sweeps and frequency shift keying (FSK) applications. Refer to <u>Features Supported</u> to determine if your device supports Frequency List mode.

The following example shows a frequency list and the generated waveform when <u>Single trigger mode</u> is selected. The <u>trigger mode</u> affects the timing and behavior of the generation.

Step	Frequency	Duration	
0	3.0 Hz	1.0 s	
1	6.0 Hz	0.9 s	
2	0.5 Hz	0.75 s	
3	9.0 Hz	1.1 s	



#### **Creating and Configuring a Frequency List**

Call the <u>niFgen Create Frequency List</u> VI or the <u>niFgen_CreateFreqList</u> function to set the function type, the frequency list, and the duration of each step in the list. You can create multiple frequency lists by making additional calls to the niFgen Create Frequency List VI or the niFgen_CreateFreqList function.

To select the active frequency list and configure the amplitude, DC offset, and start phase of the generation, call the <u>niFgen Configure Frequency</u> <u>List</u> VI or the <u>niFgen ConfigureFreqList</u> function. You can also select the active frequency list by setting the <u>Frequency List Handle</u> property or the <u>NIFGEN_ATTR_FREQ_LIST_HANDLE</u> attribute.

#### **Triggering a Frequency List**

The timing and behavior of the generation of a frequency list is dependent on the <u>trigger mode</u> you selected.

# NI 5402/5406/5441/5442 Frequency Hopping and Sweeping

You can define a frequency list for performing frequency hops and sweeps. The entire frequency list uses the same waveform loaded in the lookup memory. All steps differ with the generated frequency.



You can determine the maximum number of steps in your frequency list by querying the <u>Maximum Number Of Frequency Lists</u> property or the <u>NIFGEN_ATTR_MAX_NUM_FREQ_LISTS</u> attribute.

# **Frequency List Trigger Modes**

This topic contains information about the behavior of the signal generator in Frequency List mode with a particular trigger mode.

#### Single Trigger Mode

The device generates each step in the active frequency list sequentially. After the duration for the last step has elapsed, the signal generation stops and remains at the configured DC offset level. Only one Start trigger is required to start generation. All Start triggers after the first Start trigger are ignored.





**Note** For NI 5401/5411/5431, the last step generates continuously until the generation is aborted. All other devices remain at the configured DC offset value at the end of the duration.

#### **Continuous Trigger Mode**

The device generates the next step in the active frequency list once the duration of the step has elapsed. The frequency list repeats until generation is aborted. The frequency list generates continuously after receiving one Start trigger. All Start triggers after the first Start trigger are ignored.



#### **Stepped Trigger Mode**

The device generates the next step in the active frequency list every time a Start trigger occurs. After the duration for a step has elapsed, the signal generation stops and remains at the configured DC offset level until the next Start trigger is received. When the next Start trigger is received, the next step in the frequency list is generated. If a Start trigger is received within the specified duration of the step, the Start trigger is applied after the duration has elapsed. Any additional Start triggers received within the duration are ignored. After the final step, the frequency list repeats until generation is aborted.

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**Notes** If the <u>Trigger Source</u> property or the <u>NIFGEN_ATTR_TRIGGER_SOURCE</u> attribute is set to NIFGEN_VAL_IMMEDIATE, the only way to advance to the next step in the frequency list is to call the <u>niFgen Send Software Edge</u> <u>Trigger VI or the niFgen_SendSoftwareEdgeTrigger</u> function.

The NI 5401/5411/5431 do not support Stepped trigger mode in Frequency List mode. For these devices, Stepped trigger mode has the same behavior as Burst trigger mode.



#### **Burst Trigger Mode**

The device generates the next step in the active frequency list every time a Start trigger occurs. After the duration for a step elapses, the waveform generates until the next Start trigger is received. When the next Start trigger is received, the next step in the frequency list generates. If a Start trigger is received within the specified duration of the step, the Start trigger is applied after the duration elapses. Any additional Start triggers received within the duration are ignored.

Notes If the Trigger Source property or the NIFGEN_ATTR_TRIGGER_SOURCE attribute is set to NIFGEN_VAL_IMMEDIATE, the only way to advance to the next step in the frequency list is to call the <u>niFgen Send Software Edge</u> <u>Trigger</u> VI or the <u>niFgen_SendSoftwareEdgeTrigger</u> function.

For the NI 5401/5411/5431, the duration of the frequencies for these devices is ignored and any trigger received is applied immediately.



## NI 5402/5406/5412/5421/5422/5441/5442 Aborting Generation

You can abort the generation of the current waveform. Aborting the generation exhibits different behaviors for different <u>waveform generation</u> <u>modes</u>. Refer to <u>Features Supported</u> to determine the output modes supported by your device.

Output Mode	Abort Behavior	
Standard Function, Frequency List	Signal remains at the level for which the DC offset is configured.*	
Arbitrary Waveform, Arbitrary Sequence, Script	Signal remains at the last sample voltage level prior to the abort.	
<b>*Note</b> For the NI 5402/5406, square waveform signals drop to low when aborted.		

#### Aborting to Ground

All operation modes can abort to ground. The <u>niFgen Output Enable</u> VI or the <u>niFgen_ConfigureOutputEnabled</u> function allows you to disable the <u>output enable</u> relay to remove the DC voltage from the output.

To abort generation to ground, complete the following steps:

- 1. Disable the analog output by calling the niFgen Output Enable VI or the niFgen_ConfigureOutputEnabled function to remove any DC voltage on the analog output.
- 2. Call the <u>niFgen Abort Generation</u> VI or the <u>niFgen AbortGeneration</u> function to stop the waveform generation.

#### Aborting to a Known Voltage

Arbitrary Waveform, Arbitrary Sequence, and Script output modes can abort generation to a known voltage.

To abort the generation to known voltage, complete the following steps:

- 1. During your application, download a small, constant–amplitude waveform that corresponds to the desired output voltage. You will generate this waveform at the end of your application.
- 2. Abort generation of the current waveform.
- 3. Reconfigure the device to generate the constant–amplitude waveform. Initiate generation.
- 4. Abort the generation of the constant–amplitude waveform.

The analog output signal remains at the voltage corresponding to this waveform until the device is reconfigured for another generation.

Note Closing the NI-FGEN session to the device while generating a waveform stops the waveform generation. Stopping waveform generation at an unknown point leaves an unknown DC voltage, corresponding to the sample value when generation stopped on the CH 0 analog output connector. To ensure the output voltage goes to zero volts when closing your applications, always disable the output enable relay first and then abort the generation.

## NI 5402/5406/5412/5421/5422/5441/5442 Triggering

You can define the signal generator functionality by using the various triggering techniques. Expand this section to learn more about using triggers with your signal generator.

## NI 5402/5406 Trigger Sources

Trigger sources are software selectable. You can use any of the external input triggers as follow:

- SYNC OUT/PFI 0 or PFI 1 on the BNC front panel connectors
- RTSI<0..7> (PCI) lines or PXI_Trig<0..7> lines and PXI_Star on the PXI trigger bus on the backplane

The following figure shows the possible trigger sources for the signal generator.



#### Legend

[§]Refer to Exporting Signals for more information routing signals.

External triggers are only recognized on the rising edge of the trigger. All triggers are ignored until <u>niFgen Initiate Generation</u> VI or the <u>niFgen InitiateGeneration</u> function is called.

The default trigger source for NI-FGEN is Immediate, which causes an automatic Start trigger pulse to be generated internally as soon as hardware is ready to generate signals after generation has been initiated. You can configure the trigger source with the <u>niFgen Configure Trigger</u> (poly) VI or the <u>niFgen ConfigureTriggerSource</u> function. Refer to the <u>niFgen Send Software Edge Trigger</u> VI or the <u>niFgen_SendSoftwareEdgeTrigger</u> function for more information about

programmatically triggering the device.

Refer to the <u>module specifications</u> for the minimum Start trigger pulse width required for operation.

#### **Related Topics**

PXI Trigger Lines

PXI Star Trigger Line

## NI 5402/5406/5412/5421/5422/5441/5442 Trigger Modes

NI 5402/5406/5412/5421/5422/5441/5442 signal generators have four trigger modes: Single, Continuous, Stepped, and Burst. These trigger modes are available for Arbitrary Waveform, Arbitrary Sequence, and Frequency List output modes. Refer to the <u>niFgen Configure Trigger</u> <u>Mode</u> VI or the <u>niFgen_ConfigureTriggerMode</u> function for information about setting the trigger mode.

## NI 5402/5406/5412/5421/5422/5441/5442 Trigger Timing

The following figure shows the relationship between Start trigger and the waveform output.  $t_{s1}$  is the required pulse width on the Start trigger signal.  $t_{s2}$  is the delay from the Start trigger to the waveform output. Refer to the <u>device specifications</u> for more information about these timing parameters.



The signal generator also allows you to export signals to trigger other devices based on the waveform output of the signal generator. Two events can be exported from the signal generator to signal other devices that waveform generation has started—the exported Start trigger and the Marker event. NI-FGEN refers to the exported Start trigger as the Out Start trigger. Refer to Exporting Signals for more information about using these signals.

The exported Start Trigger event is a slightly delayed version of the Start trigger used for waveform generation. It is guaranteed to be at least 150 ns wide. The preceding figure also shows the relationship between Start trigger and the exported Start trigger.  $t_{s3}$  is the delay between the Start trigger and the time the device generates the exported Start trigger.  $t_{s4}$  is the pulse width of the exported Start trigger signal.

## NI 5402/5406/5412/5421/5422/5441/5442 Data Mask

The signal generator supports analog and digital data masks and static values. The data mask allows you to shield bits of the data to be replaced with the corresponding static value bits. For example, a mask of 0xFF00 and a static value of 0xAAAA applied to a DC waveform with a value of 0x1111 produces a DC waveform with a value of 0x11AA.

NI-FGEN supports separate and independent analog and digital data masks and static values. The analog data mask and analog static value apply to the digital data applied to the DAC, and ultimately to the signal on the analog output terminal. The analog data mask and analog static value do not affect the signals on the digital connector. For more information about analog masking, refer to the <u>Analog Data Mask</u> or <u>Analog Static Value</u> properties or the

NIFGEN_ATTR_ANALOG_DATA_MASK and

NIFGEN_ATTR_ANALOG_STATIC_VALUE attributes. The digital data mask and digital static value apply to the signals on the digital connector and they do not affect the signal on the analog output terminal. For more information about using digital masking, refer to the <u>Digital Data Mask</u> or <u>Digital Static Value</u> properties or the

<u>NIFGEN_ATTR_DIGITAL_DATA_MASK</u> and <u>NIFGEN_ATTR_DIGITAL_STATIC_VALUE</u> attributes.

## NI 5402/5406/5412/5421/5422/5441/5442 Event Delays

The NI 5402/5406/5412/5421/5422/5441/5442 signal generators support event delays that can manually delay Marker, Started, and Done events so that they are aligned on a particular Sample clock period.

Delay is applied to the event with respect to the analog output of the signal generator. For example, a delay of 0 Sample clocks aligns the event with the analog output signal, while a delay of +2 Sample clocks causes the event to appear two Sample clock periods after the analog output appears. All event delays are adjusted in increments of Sample clock periods, regardless of the units used to set the delay. For example, if you provide a value for delay with units of seconds, the delay is coerced up to the nearest Sample clock period.

The event delay attributes must be set before waveform generation is initiated. Any changes made to other attributes during waveform generation may change the analog output delay. NI-FGEN does not compensate for this change in the analog output delay, and continues to apply the event delay that you was originally configured.

If an event delay is applied to an event that is being exported to multiple output terminals, NI-FGEN aligns the event on the first terminal you specified.

For more information about setting event delays, refer to the <u>Marker</u> <u>Event Delay</u> property or the <u>NIFGEN_ATTR_MARKER_EVENT_DELAY</u> attribute, the <u>Started Event Delay</u> property or the <u>NIFGEN_ATTR_STARTED_EVENT_DELAY</u> attribute, or the <u>Done Event</u> <u>Delay</u> property or the <u>NIFGEN_ATTR_DONE_EVENT_DELAY</u> attribute.

## NI 5402/5406/5412/5421/5422/5441 Exporting Signals

The signal generator contains seven PXI trigger lines or seven RTSI (PCI devices only) lines that are available for sending signal generator-specific information to other devices that have PXI trigger or RTSI bus connectors. The signal generator also connects to the PXI Star trigger line, which you can use to send or receive signals to or from the PXI Star trigger line on an NI 6653 system timing and control module (Slot 2 controller).

 $\overline{\mathbb{N}}$ 

**Note** For more information about the NI 6653 system timing and control module, visit ni.com/products.

The signal generator has connectors on the front panel to route signals to devices external to the PXI or PCI chassis. The following table shows the signals available for export and the lines they can be routed to. To determine all possible signal routes for your device, refer to <u>Signal</u> <u>Routing</u>.

		Destination		
		PXI Bus, PXI_Trig<06>, RTSI Bus, RTSI<06>, or PXI_STAR	SYNC OUT/PFI 0 and PFI 1 Connectors	PFI<45>* on DIGITAL DATA & CONTROL Connector
	Sample Clock	Yes	Yes**	_
Exported	Sample Clock Timebase***	Yes	Yes	_
Clocks, Triggers, and Events	PLL Reference Source	Yes	Yes**	_
	Out Start	Yes	Yes	Yes

	trigger			
	Marker Event	Yes	Yes***	Yes
*Nete Devices without a DDC connector are not supported				

****Note** Devices without a DDC connector are not supported. ****Note** SYNC OUT/PFI 0 is optimized for the Sample clock and PLL reference source signals and has slightly less jitter than PFI 1. SYNC OUT/PFI 0 is the recommended terminal to use for exporting clocks. *****Note** This configuration is not supported on the NI 5402/5406.

**Sample Clock**–The clock signal that tells the DAC when to convert the digital waveform values to an analog voltage. The Sample clock frequency is referred to as the Sample clock rate; the rate at which the digital waveforms from device memory are generated. The Sample clock is also known as update clock.



**Notes** The Sample clock can be exported directly, or it can first be divided down by an integer. This configuration provides a variable frequency signal related to the waveform sample rate to synchronize other devices to the generation.

NI does not recommend exporting clocks greater than 20 MHz over PXI_TRIG<0..6> or RTSI<0..6>.

If you export the divided-down Sample clock to another device to synchronize sampling, you can also use the Sample clock as the Start trigger for the signal generator. Using the divided-down Sample clock as the Start trigger begins signal generation at the same place each time relative to the divided-down Sample clock. This technique is more useful as the divisor becomes larger and, while an improvement over using an immediate Start trigger, there remains an uncertainty of one Sample clock.

**Sample Clock Timebase**–The clock signal from which the internal Sample clock is derived. For the NI 5402/5406/5412/5421/5441, the Sample clock timebase is 100 MHz; for the NI 5422, the Sample clock timebase is 200 MHz. The Sample clock timebase is also know as board clock.



**Note** The Sample clock timebase (board clock) is always exported after being divided-down. The default divide-down value is 2 for

the NI 5412/5421/5441 and 4 for the NI 5422. Valid divide-down values range from 2 to 4,194,304 for the NI 5412/5421/5441 and 4 to 4,194,304 for the NI 5422.

If you export the Sample clock timebase to another device to synchronize sampling, you can also use the Sample clock timebase as the Start trigger for the signal generator. Using the Sample clock timebase as the Start trigger begins signal generation at the same place each time relative to the Sample clock timebase. This technique is more useful as the divisor becomes larger and while an improvement over using an immediate Start trigger there remains an uncertainty of one Sample clock.

**PLL Reference source**–A clock signal that is only available when a PLL Reference source has been configured. The clock is the source selected as the PLL Reference Clock source.

**Out Start trigger**–A signal generated by the device upon recognizing a start condition that can be routed out various connectors to signal other devices.

**Marker event**–A digital signal that can be used as a trigger corresponding to a specific sample in the waveform generation. This signal controls other devices that require timing information related to a specific point in the generated waveform.

#### **Routing Signals**

You can route signals in the following ways:

- The Marker event generated during an Arbitrary Waveform Generation mode waveform generation to any of the PXI trigger lines, RTSI lines (PCI devices only), PXI_STAR, or front panel connectors.
- The signal generator Start trigger output signal to other devices through any of the PXI trigger lines, RTSI lines (PCI devices only), PXI_STAR, or front panel connectors.
- The signal generator Sample clock signal to other devices through any of the PXI trigger lines, RTSI lines (PCI devices only), PXI_STAR, or front panel connectors.
- The PLL Reference clock source to other devices through any of the PXI trigger lines, RTSI lines (PCI devices only), PXI_STAR, or front panel connectors.

In NI-FGEN, the PXI trigger lines are referred to as RTSI<0..6>. The correlation between PXI_TRIG<*x*> and RTSI<*x*> is one to one. For more information about configuring and routing the device internal signals, refer to the <u>niFgen Export Signal</u> VI or the <u>niFgen ExportSignal</u> function.

## NI 5402/5406/5412/5421/5422/5441/5442 Synchronization

Your signal generator is based on the <u>National Instruments</u> <u>Synchronization and Memory Core (SMC)</u> technology and therefore supports TClk synchronization. Refer to the <u>NI-TClk Synchronization</u> <u>Help</u> for more information about NI-TClk Synchronization.

#### NI 5402/5406/5412/5421/5422/5441/5442 Specifications

For information about the signal generator specifications, refer to the <u>device specifications</u>. You can access these specifications by navigating to **Start»All Programs»National Instruments»NI-FGEN»Documentation»Hardware Specifications**, or you can visit <u>ni.com/manuals</u>.

## NI 5402/5406/5412/5421/5422/5441/5442 Calibration

Before shipping your signal generator, NI calibrated your device to ensure that all features are within specifications.

Calibration is a set of operations that compares the values indicated by a measuring instrument or measuring system to the corresponding values realized by external standards. You can use the results of calibration to determine the measurement error and can then correct for it in the adjustment process.

The calibration process consists of verifying, adjusting, and reverifying a device. During verification, you compare the measured performance to an external standard of known measurement uncertainty to confirm that the product meets or exceeds specifications. During adjustment, you correct the measurement error of the device by adjusting the calibration constants and storing the new calibration constants in the EEPROM. The host computer reads the calibration constants and the software uses them to compensate for errors in the data and to present calibrated data to the user.

For more information about calibrating the signal generator, refer to the <u>device calibration</u> procedures.

For more information about calibration in general, refer to <u>ni.com/calibration</u>.
# Accessories

National Instruments offers a variety of products to use with your signal generator, including cables and other accessories. Visit <u>ni.com</u> for more information.

## NI PCI-5402/5406 Front Panel

The following figure shows the NI PCI-5402/5406 front panel. This front panel has four BNC connectors.



The  $\underline{CH 0}$  connector is the analog output from which arbitrary waveforms are generated.

The <u>REF IN</u> connector provides the device with an external reference or external Sample clock.

The <u>SYNC OUT/PFI 0 and PFI 1</u> connectors are multi-directional connections for a number of different signals.

#### NI PXI-5404 Overview

The NI 5404 is a 100 MHz frequency generator with the following features:

• A 0 MHz to 105 MHz SINE out with adjustable amplitude from 1  $V_{pk-pk}$  to 2  $V_{pk-pk}$  into a 50  $\Omega$  load

Note The SINE amplitude begins to fall off below 9 kHz.

• A 0 MHz to 105 MHz <u>CLOCK</u> out with 5 V, 3.3 V, or 1.8 V adjustable amplitude levels into high impedance load



- **Note** The CLOCK output is a TTL version of the SINE output; thus, the two connectors cannot generate different frequencies.
- Phase-locked looping to an external Reference clock
- Synchronization of board outputs to an external trigger
- External calibration to establish onboard clock frequency accuracy, sine amplitude accuracy, and square wave duty cycle accuracy

## NI PXI-5404 Connecting Signals

The following figure shows the NI PXI-5404 front panel. The front panel contains five SMB connectors. The sine output generates through the connector labeled <u>SINE</u>, and the clock output generates through the connector labeled <u>CLOCK</u>.



## NI PXI-5404 SINE Out

The SINE out provides the sine wave output. The maximum output levels on this connector depend on the type of load termination. If the output of the NI PXI-5404 terminates into a 50  $\Omega$  load, the output levels are adjustable to a maximum of ±1 V, as shown in the following figure.



If the output of the NI PXI-5404 terminates into a high-impedance load (HiZ), the output levels are adjustable to a maximum  $\pm 2$  V. If the output terminates into any other load, the levels are as follows:

 $V_{out} = \pm [R_L / (R_L + R_O)] \times 2 V$ 

where

 $V_{out}$  is the maximum output voltage level.

 $R_L$  is the load impedance in ohms.

 $R_{\rm O}$  is the output impedance on the NI PXI-5404 and is equal to 50  $\Omega$ .



Note Software sets the voltage output levels assuming a 50  $\Omega$  load termination.

## NI PXI-5404 CLOCK Out

CLOCK out provides the clock output. The maximum output levels on this connector depend on the type of load termination. If the CLOCK out of the NI PXI-5404 terminates into a high-impedance load (HiZ), you can configure the output levels with the software to 5 V, 3.3 V, or 1.8 V, as shown in the following figure. Therefore, the maximum level is 5 V.



If the CLOCK out of the NI PXI-5404 terminates into a 50  $\Omega$  load, the output levels are 2.5 V, 1.65 V, or 0.9 V. Thus, the maximum level you can obtain is 2.5 V. If the output terminates into any other load, the levels are as follows:

 $V_{out} = [R_L / (R_L + R_O)] \times 5 V$ 

where

 $V_{out}$  is the maximum output voltage level.

 $R_L$  is the load impedance in ohms.

 $R_{O}$  is the output impedance on the NI PXI-5404 and is equal to 50  $\Omega$ .

By default, the CLOCK out is set to 5 V into HiZ, but you can use software to set it to 3.3 V or 1.8 V into HiZ.



**Note** Software sets the voltage output levels assuming a HiZ load termination.

#### NI PXI-5404 PFI 0 Connector

The PFI 0 connector is a bi-directional connector. As an input, the PFI 0 connector can accept a trigger from an external source that can start waveform generation. As an output, the PFI 0 connector can route out a signal from the following sources:

- CLOCK out
- Divided-down Sample clock timebase (20 MHz by default, derived from VCXO generated clock)
- REF IN connector
- PXI 10 (backplane clock)
- Software trigger
- PXI Star trigger
- PXI trigger bus (RTSI) lines

An input trigger should have values of  $V_{IH}$  = 2.0 V and of  $V_{IL}$  = 0.8 V.

The output trigger has values of  $V_{OH}$  = 4.07 V and of  $V_{OL}$  = 0.44 V into HiZ.

## NI PXI-5404 REF OUT Connector

The REF OUT connector is an output connector that can route out a signal from the following sources:

- CLOCK out
- Divided-down Sample clock timebase (20 MHz by default, derived from VCXO generated clock)
- REF IN connector
- PXI 10 (backplane clock)
- Software trigger
- PXI Star trigger
- PFI 0 connector
- PXI trigger bus (RTSI lines)

The output clock has values of  $V_{OH}$  = 4.07 V and of  $V_{OL}$  = 0.44 V into HiZ. Rise and fall time for the output clock is 2.4 ns.

#### NI PXI-5404 REF IN Connector

The REF IN connector is a PLL input connector that can accept a Reference clock from an external source and frequency lock the NI 5404 internal clock to this external clock. The Reference clock can be 3 MHz to 20 MHz in 1 MHz steps. The clock should not deviate more than ±50 ppm from its nominal frequency. You can use a sine wave or a square wave from 250 mV_{pk-pk} to 5 V_{pk-pk} as the Reference clock.



**Note** You can frequency lock the NI 5404 to other NI devices using the 10 MHz backplane clock.

If an external Reference clock is not available, the NI 5404 automatically tunes the internal clock to the highest accuracy possible.

#### NI PXI-5404 LEDs

The NI PXI-5404 has two LEDs to indicate status: ACCESS and ACTIVE.

#### ACCESS LED

The ACCESS LED indicates basic hardware status.

Color	Indications
Off	Device is not ready, not yet functional, or the device has detected a problem with a power rail.
Amber	Amber indicates that the device is being accessed.
Green	The device is ready to be programmed by a driver.

#### ACTIVE LED

The ACTIVE LED indicates the state of the device.

Color	Indications
Off	Device is disabled or in a stopped state.
Amber	Indicates that the device is armed and waiting for a Start trigger. Also used to indicate that a device is paused.
Green	Indicates that the device is generating a waveform.
Red	The device has detected an error. Software must access the device to determine the cause of the error. The LED remains red until the error condition is removed. Some example errors are:
	<ul> <li>PLL Unlocked—The device has detected an unlocked condition on a previously locked PLL. A PLL that is unlocked while in reset, or the device is still in a power-up state.</li> <li>Software detected an error.</li> </ul>

# NI PXI-5404 Power-Up and Reset Conditions

When you power up the computer, the NI PXI-5404 is in the following state:

- The outputs do not have a signal.
- REF IN and PFI 0 connectors are not functional and do not react to any input signals.

When you reset the device using NI-FGEN, the NI PXI-5404 is in the following state:

- The device is stopped (not generating).
- The SINE and CLOCK output terminals are enabled, but no signal is seen because the device is not generating.
- CLOCK and SINE output amplitudes are set to their maximum values.
- CLOCK and SINE frequencies are set to 1 MHz.
- The PLL reference source is set to internal tuning (the VCXO is not locked to an external reference signal).
- The CLOCK duty cycle is set to 50%.
- Trigger source is set to immediate.

## NI PXI-5404 Theory of Operation

Expand this topic for information about the NI 5404 theory of operation.

## NI PXI-5404 Block Diagram

The following figure shows the NI PXI-5404 block diagram.



## NI PXI-5404 Analog Output

Analog waveforms are generated by the following process:

- 1. The direct digital synthesis output high-speed DAC receives the 12-bit digital waveform data from the direct digital synthesis chip.
- 2. A lowpass filter filters the direct digital synthesis output.
- 3. This filtered signal passes through the first amplification stage and then passes to a comparator to generate the <u>CLOCK</u> out on the front panel.
- 4. The amplified signal also passes through another amplification stage.
- 5. The final amplified signal gets AC coupled and goes to the <u>SINE</u> out.

Refer to the <u>NI PXI-5404 Block Diagram</u> for more information about analog waveform generation.

The following figure shows the timing relationships of the trigger input and waveform output.  $t_{d1}$  is the pulse width on the trigger signal.  $t_{d2}$  is the time delay from trigger to output on the <u>SINE</u> out.



## NI PXI-5404 Locking to a Reference Clock

The onboard clock of the NI PXI-5404 can be locked to an external reference signal. This can be used when synchronizing multiple NI 5404 signal generators or whenever the output frequency needs to be locked to some external source. If no reference source is specified, the device will use an internal reference that can be adjusted during a device calibration.

The Reference clock source can be configured using the <u>niFgen</u> <u>Configure Reference Clock VI or the niFgen_ConfigureReferenceClock</u> function or by setting the <u>Reference Clock Source</u> property or <u>NIFGEN_ATTR_REF_CLOCK_SOURCE</u> attribute directly. In addition to specifying the source of the Reference clock signal, you must also specify its frequency. The Reference clock frequency can be configured using the <u>niFgen Configure Reference Clock</u> VI or the <u>niFgen_ConfigureReferenceClock</u> function or by setting the <u>Reference</u> <u>Clock Frequency</u> property or the

<u>NIFGEN_ATTR_REF_CLOCK_FREQUENCY</u> attribute directly. The NI PXI-5404 can lock to 3 MHz to 20 MHz frequencies (in 1 MHz steps).

Reference Source	Description
NIFGEN_VAL_REF_CLOCK_INTERNAL	No external reference is used. The device uses an internal reference.
NIFGEN_VAL_PXI_CLK10	10 MHz PXI backplane clock.
NIFGEN_VAL_REF_IN	REF IN connector on the NI 5404 front panel.
NIFGEN_VAL_RTSI_<06>	One of the RTSI/PXI trigger lines
NIFGEN_VAL_REF_CLOCK_RTSI_CLOCK	RTSI clock line (RTSI_7/PXI_Trig7)

The following table lists the NI-FGEN synchronization examples for various ADEs.

ADE	
LabVIEW	<labview>\examples\instr\niFgen\niFgen_5404_Synchron</labview>
LabWindows/CVI	<cvi>\Samples\niFgen\Synchronization5404.prj</cvi>
C++	<measurementstudio>\VC\Examples\niFgen\niFgen_5404_</measurementstudio>
Visual Basic	<measurementstudio>\VB\Samples\niFgen\5404_Synchron</measurementstudio>
Standard C	<program files="">\IVI\Drivers\niFgen\Examples\c\Synchroniz</program>

#### NI PXI-5404 Phase-Locked Looping

The NI PXI-5404 has a PLL that optionally phase-locks the device clock to a Reference clock. With the NI PXI-5404, you can phase-lock to the PXI backplane clock, an external Reference clock that is brought in through the REF IN front panel connector, or a clock brought in from practically any other source. If you use an external clock, the nominal value of the frequency must be 10 MHz and the frequency must be within 100 ppm of 10 MHz. When phase-locking is disabled, the voltage from a DAC determines the frequency of the device clock. The value of this voltage provided by the DAC is established during factory calibration. The following figure shows the components and possible configurations of the phase-locking circuitry.



1Also Called P XI 10

## NI PXI-5404 Waveform Generation

The NI 5404 frequency generator can generate sine or square waves at frequencies between 0 MHz and 105 MHz. NI-FGEN supports the NI 5404 in Standard Function mode only (the <u>Output Mode</u> property and the <u>NIFGEN_ATTR_OUTPUT_MODE</u> attribute can only be set to NIFGEN_VAL_OUTPUT_FUNC). In the standard function output mode, you can configure the following waveform properties: <u>Waveform</u>, Frequency, Amplitude, DC Offset, Start Phase, and Duty Cycle High (NIFGEN_ATTR_FUNC_WAVEFORM, NIFGEN_ATTR_FUNC_FREQUENCY, NIFGEN_ATTR_FUNC_AMPLITUDE, NIFGEN_ATTR_FUNC_OC_OFFSET, NIFGEN_ATTR_FUNC_START_PHASE, and <u>NIFGEN_ATTR_FUNC_DUTY_CYCLE_HIGH</u> attributes, respectively). You can configure many of these properties and attributes using the niFgen Configure Standard Waveform VI or the

<u>niFgen_ConfigureStandardWaveform</u> function.

The waveform output terminals on the NI 5404, <u>SINE</u> out and <u>CLOCK</u> out, are closely related. The TTL signal at CLOCK out is derived from the sine wave. Therefore, the two terminals are treated as the same channel in NI-FGEN. Enabling and disabling the output affects both terminals. When the frequency and phase properties or attributes are set, both terminals are affected simultaneously. You can set amplitude and duty cycle on each terminal independently (DC offset can be read but not set). When you set or get one of these properties or attributes, the result depends on the value of the Waveform property or the NIFGEN_ATTR_FUNC_WAVEFORM attribute.

The Waveform property or the NIFGEN_ATTR_FUNC_WAVEFORM attribute determines which terminal is being configured when you set certain properties or attributes. When the waveform is set to a sine wave (the <u>Waveform</u> property or the <u>NIFGEN_ATTR_FUNC_WAVEFORM</u> attribute is set to NIFGEN_VAL_WFM_SINE), setting the amplitude configures the output of SINE out. Accordingly, if the waveform is set to a square wave (NIFGEN_VAL_WFM_SQUARE), you can configure the

amplitude and duty cycle of the TTL signal at the CLOCK out. The settings specific to each terminal are preserved when the Waveform property or the NIFGEN_ATTR_FUNC_WAVEFORM attribute is changed, so both SINE out and CLOCK out can be configured separately in the same session.

#### **Related Topics**

<u>Generating a Sine Wave</u> <u>Generating a Clock Signal (Square Wave)</u> <u>Locking to a Reference Clock</u> <u>Routing/Exporting Signals</u>

## NI PXI-5404 Start Conditions

#### SINE Out

The sine waveform is configured by three parameters: frequency, amplitude, and phase. All the parameters are sent to the direct digital synthesis chip at the same time; however, because of delays within the chip, the phase and amplitude are set before the frequency. The result of these delay differences is a DC voltage at the SINE out before the sine signal appears. The duration of this DC signal is about 100 ns, and its level depends on the given phase and amplitude. You can see this start up condition for different phase settings in the following figures.



Sine Output Starting for Phase Set to 45 Degrees



Sine Output Starting for Phase Set to 90 Degrees

Because a phase of  $0^{\circ}$  or  $180^{\circ}$  corresponds to a starting amplitude of 0 V, you can use one of these two phase settings to eliminate this particular start up condition. Refer to the following figure for an example of a start phase of  $0^{\circ}$ .

 $0 \vee -$ 

#### Sine Output Starting for Phase Set to 0 Degrees

In addition, when generating higher frequencies, a runt pulse exists upon start-up. Refer to the following figure for an example of a runt pulse.

οv

Runt Pulse on SINE Output When Starting at a High Frequency for Phase Equal to Zero

#### **CLOCK Out**

The start condition of the CLOCK out depends on the start phase of the SINE out. Therefore, a runt pulse may occur upon starting the clock. Refer to the following figure for an example of a runt pulse.



#### Runt Pulse on Start-up of CLOCK Output for Phase Equal to Zero

For certain phase settings, the runt pulse does not occur. To eliminate the runt pulse on the CLOCK out, experiment with the starting phase setting.

Also, because of the different output paths of the CLOCK out and SINE out, a fixed delay exists after the SINE out initiates until the CLOCK out initiates.

# NI PXI-5404 Generating a Sine Wave

Complete the following steps to generate a sine wave with the NI PXI-5404

- 1. Initialize an NI-FGEN session to the appropriate device (<u>niFgen</u> <u>Initialize</u> VI or <u>niFgen_init</u> function).
- 2. Set the appropriate standard function properties or attributes for the desired generation.

Property	Attribute	Value
<u>Waveform</u>	NIFGEN_ATTR_FUNC_WAVEFORM	NIFGEN_VAL_V
Frequency	NIFGEN ATTR FUNC FREQUENCY	Desired frequent
Amplitude	NIFGEN ATTR FUNC AMPLITUDE	Desired amplituc
		into a 50 $\Omega$ load)
		to 2 V _{pk-pk}

- 3. Initiate the generation (<u>niFgen Initiate Generation</u> VI or <u>niFgen InitiateGeneration</u> function). The sine wave should be generated at the SINE Out terminal.
- If you want to stop the generation, do so by disabling the output (<u>niFgen Output Enable</u> VI or <u>niFgen_ConfigureOutputEnabled</u> function) and/or aborting the generation (<u>niFgen Abort Generation</u> VI or <u>niFgen_AbortGeneration</u> function).
- 5. Close the NI-FGEN session (<u>niFgen Close</u> VI or <u>niFgen_close</u> function).

The following table lists the NI-FGEN sine wave example for various ADEs.

ADE	Path
LabVIEW	<pre><labview>\examples\instr\niFgen\niFgen_5404_Sine_Ger</labview></pre>

LabWindows/CVI	<cvi>\Samples\niFgen\SineGeneration5404.prj</cvi>
Measurement Studio C++	<measurementstudio>\VC\Examples\niFgen\niFgen_5404_</measurementstudio>
Visual Basic	<measurementstudio>\VB\Samples\niFgen\5404_Sine_Exa</measurementstudio>
Standard C	<program files="">\IVI\Drivers\niFgen\Examples\c\SineGener</program>

# NI PXI-5404 Generating a Clock Signal (Square Wave)

- 1. Initialize an NI-FGEN session for the appropriate device (<u>niFgen</u> <u>Initialize</u> VI or <u>niFgen_init</u> function).
- 2. Set the appropriate standard function properties or attributes for the desired generation.

Properties	Attribute	
<u>Waveform</u>	NIFGEN ATTR FUNC WAVEFORM	NIFGEN
<u>Frequency</u>	NIFGEN ATTR FUNC FREQUENCY	the desi 0 MHz t
Amplitude	NIFGEN_ATTR_FUNC_AMPLITUDE	the desi into a hi 1.8 V, 3.
<u>Duty Cycle</u> High	NIFGEN ATTR FUNC DUTY CYCLE HIGH	The des legal val frequenc

- 3. Initiate the generation (niFgen_InitiateGeneration). The square wave should be generated at CLOCK out.
- If you want to stop the generation, do so by disabling the output (<u>niFgen Output Enable</u> VI or <u>niFgen_ConfigureOutputEnabled</u> function) and/or aborting the generation (<u>niFgen Abort Generation</u> VI or <u>niFgen_AbortGeneration</u> function).
- 5. Close the NI-FGEN session (<u>niFgen Close</u> VI or <u>niFgen_close</u> function).

The following table lists the NI-FGEN clock signal (square wave) example for various ADEs.

LabVIEW	<labview>\examples\instr\niFgen\niFgen_5404_Clock_G</labview>
LabWindows/CVI	<cvi>\Samples\niFgen\ClockGeneration5404.prj</cvi>
C++	<measurementstudio>\VC\Examples\niFgen\niFgen_5404_</measurementstudio>
Visual Basic	<measurementstudio>\VB\Samples\niFgen\5404_Clock_Ex</measurementstudio>
Standard C	<program files="">\IVI\Drivers\niFgen\Examples\c\ClockGene</program>

# NI PXI-5404 Triggering

NI-FGEN allows you to start generation immediately. You can also use a software trigger or an external digital trigger. If you configure the generation to start immediately, the waveform outputs as soon as the niFgen Initiate Generation VI or the niFgen_InitiateGeneration function is called. If you specify a software trigger, the generation does not start as soon as Initiate Generation is called; instead the generation waits until the niFgen_SendSoftwareEdgeTrigger function is called. If you specify an external trigger, the generation does not begin until a rising edge is detected on the specified source terminal.

You can configure the trigger source by calling the <u>niFgen Configure</u> <u>Trigger (poly)</u> VI or the <u>niFgen ConfigureDigitalEdgeStartTrigger</u> <u>niFgen_ConfigureSoftwareEdgeStartTrigger</u> functions or by setting the <u>Trigger Source</u> property or the <u>NIFGEN ATTR TRIGGER SOURCE</u> attribute directly. You can change standard function properties or attributes, such as frequency, phase, and amplitude, while generating a waveform. If you configure the generation to trigger immediately, the change takes effect as soon as the property or attribute is changed. If you trigger the generation using software or an external digital trigger, the change does not take effect until the next trigger is received. For example, imagine that the trigger source is a software trigger and a generation is in progress. If you change the <u>Frequency</u> property or the <u>NIFGEN_ATTR_FUNC_FREQUENCY</u> attribute, the output frequency does not actually change until you call the niFgen Send Software Edge Trigger VI or the niFgen_SendSoftwareEdgeTrigger function again.

Trigger	Source Description
NIFGEN_VAL_IMMEDIATE	No trigger is used. Generation starts and updates happen immediately.
NIFGEN_VAL_SOFTWARE_TRIG	The software trigger function call.
NIFGEN_VAL_PFI_0	The PFI 0 connector on the NI 5404 front panel.
NIFGEN_VAL_RTSI_<07>	One of the RTSI/PXI trigger lines.

NIFGEN_VAL_PXI_STAR

# NI PXI-5404 Trigger Sources

By default, the NI PXI-5404 starts immediately, after initiating a generation in software, unless a trigger is selected. When you use the Start trigger option, you can software select from one of the following sources:

- PXI trigger bus (RTSI) line
- PFI 0 (front panel connector)
- PXI Star
- Software trigger

The following figure shows the trigger sources for the NI 5404.



#### **Waveform Generation Trigger Sources**

If you need to automatically trigger the waveform generation, use software to generate the triggers. You need a rising TTL edge for external triggering.

For external triggering, apply a rising-edge TTL signal to the PFI 0 input. This signal should remain de-asserted (logic low) until after the software has initialized the waveform generation.

## NI PXI-5404 RTSI/PXI Trigger Lines

The NI PXI-5404 allows for a variety of signals to be routed to, and from, the PXI trigger (RTSI) lines.

As a source, these lines can be sent to the PFI 0 connector and used to trigger other devices in the system. You can also route RTSI lines to the REF OUT connector and use them to provide a clock to other devices. Additionally, any of these lines can be routed to other RTSI lines.

The following figure shows all the routes for RTSI lines.



As a sink, RTSI lines can receive the following:

- Start trigger
- Divided-down, onboard clock (20 MHz by default)
- Software trigger
- <u>REF IN</u>
- PXI 10
- PXI Star
- PFI 0
- <u>CLOCK</u>
- Other RTSI lines

The following figure describes all the possible routes with the RTSI lines at the sink of the route.





**Note** RTSI lines may not receive signals of frequencies higher than 20 MHz. When the divided-down, onboard clock (*BOARD CLOCK/N*) is routed to these lines, *N* should be  $\geq$  3. *N* is 3 by default.

# NI PXI-5404 Trigger Mode

The NI 5404 has only one trigger mode: <u>Continuous</u>.
# NI PXI-5404 Routing/Exporting Signals

Many different signals can be routed and exported from the NI PXI-5404. A route is made using <u>niFgen Route Signal Out</u> VI or the <u>niFgen_RouteSignalOut</u> function by specifying the desired source signal or terminal and the desired destination terminal.

Source	Description
NIFGEN_VAL_NONE	Routes nothing to the destination terminal—effectively clears any routes to the terminal
NIFGEN_VAL_CLOCK_OUT	CLOCK out signal
NIFGEN_VAL_OUT_START_TRIGGER	Start trigger signal
NIFGEN_VAL_SOFTWARE_TRIG	Signal generated by <u>niFgen</u> <u>Send Software Edge Trigger</u> VI or <u>niFgen_SendSoftwareEdgeTrigger</u> function
NIFGEN_VAL_BOARD_CLOCK	20 MHz signal derived from the Sample clock timebase
NIFGEN_VAL_REF_IN	REF IN connector on the NI 5404 front panel
NIFGEN_VAL_PXI_CLK10	10 MHz PXI backplane clock
NIFGEN_VAL_PXI_STAR	PXI Star trigger line
NIFGEN_VAL_PFI_0	PFI 0 connector on the NI 5404 front panel
NIFGEN_VAL_RTSI_<07>	One of the RTSI/PXI trigger lines

The following table lists the signal sources for the NI 5404.

The following table lists the destination of signals from the NI 5404.

Destination	Description
NIFGEN_VAL_REF_OUT	REF OUT connector on the NI 5404 front panel

NIFGEN_VAL_PFI_0	PFI 0 connector on the NI 5404 front panel
NIFGEN_VAL_RTSI_<07>	One of the RTSI/PXI trigger lines
NIFGEN_VAL_REF_CLOCK_RTSI_CLOCK	RTSI_CLOCK line (RTSI/PXI_7)

# NI PXI-5404 Phase-Locked Loop and Module Synchronization

The NI PXI-5404 has an onboard, voltage-controlled crystal oscillator (VCXO) with a tuning range of ±50 ppm. The VCXO generates the main clock of 60 MHz. You can lock the PLL to a Reference clock source from the external REF IN connector, from any of the PXI trigger bus (RTSI) lines or from the 10 MHz backplane clock.

The PLL circuitry divides both the VCXO and the Reference clock down to 1 MHz. A phase comparator then compares the two 1 MHz signals and sends out an error signal. This error signal is filtered and sent to the control pin of the VCXO whose frequency gets adjusted. To achieve phase-locked looping correctly, the external Reference clock must be a multiple of 1 MHz and should have a frequency error of no more than ±50 ppm. The REF IN connector handles frequencies from 3 MHz to 20 MHz and amplitudes from 250 mV_{pk-pk} to 5 V_{pk-pk}.

The following figure shows the block diagram for the NI 5404 device PLL circuit.





**Caution** Do *not* increase the voltage level of the clock signal at the REF IN connector by more than the specified limit,  $5 V_{pk-pk}$ .

Note If you lock two or more NI 5404 signal generators to each other using the same Reference clock, they are frequency locked, but the initial phase relationship is indeterminate. You can adjust phase programmatically after the generation is initiated.

# NI PXI-5404 Specifications

For information about the NI PXI-5404 specifications, refer to the <u>Specifications for the NI PXI-5404</u>. You can access these specifications by navigating to **Start»All Programs»National Instruments»NI-FGEN»Documentation»Hardware Specifications**, or you can visit <u>ni.com/manuals</u>.

### NI PXI-5404 Calibration

Before shipping you the NI PXI-5404, NI calibrated your device to ensure that all features are within specifications.

Calibration is a set of operations that compares the values indicated by a measuring instrument or measuring system to the corresponding values realized by external standards. The result of calibration can be used to determine the measurement error and can correct for it in the adjustment process.

The calibration process consists of verifying, adjusting, and reverifying a device. During verification, you compare the measured performance to an external standard of known measurement uncertainty to confirm that the product meets or exceeds specifications. During adjustment, you correct the measurement error of the device by adjusting the calibration constants and storing the new calibration constants in the EEPROM. The host computer reads the calibration constants and the software uses them to compensate for errors in the data and to present calibrated data to the user.

For more information about calibrating NI signal generators, refer to <u>ni.com/calibration</u>.

# NI PXI-5404 Accessories

National Instruments offers a variety of probes and cables to use with NI PXI-5404 signal generators.

The following table lists recommended part numbers for cables that you can use with the NI PXI-5404.

Device	Cable	Part Number	Cable Description
NI PXI- 5404	SMB 110	763405-01	50 $\Omega$ SMB male to BNC male, 1 m coaxial cable
NI PXI- 5404	SMB 300	763388-01	50 $\Omega$ SMB male to alligator clip, 1 m cable

For more information about these products, visit <u>ni.com</u>.

### NI PCI/PXI 5411 Overview

The NI 5411 is a 40 MS/s arbitrary waveform generator with the following features:

- One 12-bit resolution output channel
- Up to 16 MHz sine and transistor-transistor logic (TTL) waveform output for the NI 5411
- Up to 1 MHz square, triangle, ramp up, and ramp down, as well as DC and noise
- Software-selectable output impedances of 50  $\Omega$  and 75  $\Omega$  output attenuation levels from 0 dB to 73 dB
- Phase-locked loop (PLL) synchronization to external clocks
- Sampling rate up to 40 MS/s
- Up to 8,000,000-sample onboard waveform memory
- Waveform linking and looping for arbitrary waveform generation
- Digital and analog filters
- The Function Generation mode is implemented with 32-bit direct digital synthesis (DDS)
- External trigger input
- Marker as trigger output
- 16-bit digital pattern generation with clock
- Real-Time System Integration (RTSI) and PXI triggers

All NI 5411 signal generators follow industry-standard Plug and Play specifications on both buses and offer seamless integration with compliant systems. If the application requires more than one channel of arbitrary waveform generation, you can synchronize multiple devices on all platforms using RTSI/PXI bus triggers on devices that use the RTSI/PXI bus or the digital trigger on the I/O connector.

# NI PXI/PCI-5411 Front Panel Connectors

The following figure shows the NI PXI/PCI-5411 front panels. The NI PXI-5411 front panel contains six connectors—two BNC connectors, three SMB connectors, and one 50-pin digital connector. The NI PCI-5411 has four connectors—three SMB connectors and 50-pin digital connector.



# NI PXI/PCI-5411/5431 **ARB/VIDEO OUT Connector**

The ARB/VIDEO OUT connector provides the waveform output. The maximum output levels on this connector depend on the type of load termination. If the output of the NI PXI/PCI-5411/5431 terminates into a 50  $\Omega$  load, the output levels are ±5 V, as shown in the following figure.



If the output of the NI PXI/PCI-5431 terminates into a high-impedance load (HiZ), the output levels are  $\pm 10$  V. If the output terminates into any other load, the levels are as follows:

 $V_{out} = \pm [R_1 / (R_1 + R_0)] \times 10 V$ 

where

Vout is the maximum output voltage level

 $R_1$  is the load impedance in ohms

 $R_{O}$  is the output impedance on the NI PXI/PCI-5411/5431

By default,  $R_{\Omega}$  = 50  $\Omega$ , but you can use software to set it to 75  $\Omega$ .

N Note The voltage output levels are set in the software based on a 50  $\Omega$  load termination. If you are using the NI PXI/PCI-5431, you should use software to select  $R_{\Omega}$  = 75  $\Omega$  for video generation.

For more information, refer to waveform generation and analog output operation. For specifications on the waveform output signal, refer to the NI 5411/5431 Specifications.



**Caution** Do not set the output voltage level for the NI PXI/PCI-5431 to more than  $\pm 1$  V into 75  $\Omega$ , because doing so may damage the video display module or the DUT. Always check the output levels before connecting a DUT to the NI PXI/PCI-5431. National

Instruments is not responsible for any damage caused to the DUT.

# NI PXI/PCI-5411/5431 PLL Ref/External Clock Connector

The PLL Ref/External Clock connector on the NI 5411/5431 has different uses depending on which NI 5411/5431 you are using.

#### • NI PCI-5411

The PLL Ref connector is a phase-locked loop (PLL) input connector that can accept a Reference clock from an external source and phase lock the NI PCI-5411 internal clock to this external clock. The Reference clock should not deviate more than ±100 ppm from its nominal frequency. The minimum amplitude levels of 1 V_{pk-pk} are required on this clock. You can lock Reference clock frequencies of 1 MHz and 5–20 MHz in 1 MHz steps.

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Note You can phase lock the NI PCI-5411 to other NI devices over the RTSI bus using the 20 MHz RTSI clock signal. You can phase lock the NI PXI-5411 to other NI devices using the 10 MHz backplane clock.

If no external Reference clock is available, the NI 5411 automatically tunes the internal clock to the highest accuracy possible. For more information about PLL operation, refer to <u>Phase Locked Loops and</u> <u>Module Synchronization</u>.

#### • NI PCI-5431

You can use the PLL Ref/External Clock connector for phase locking to an external source when the device is not in video mode. The device timing circuit in video mode does not support phase-lock looping. However, if the PLL reference frequency is suitable for video generation, you can generate a video waveform with the device in normal Arbitrary Waveform Generation mode.

#### • NI PXI-5411/5431

In addition to phase locking (on the NI 5411), the PLL REF/External Clock connector also provides input from an external Sample clock. You can select this functionality on the NI 5411/5431 through the software. You can feed a TTL/CMOS-level clock to this connector with a maximum frequency of 40 MHz.



**Caution** You must not change the external clock while waveform generation is in progress. Only modify the frequency of the external clock before you start the waveform generation or after you stop the waveform generation. NI cannot guarantee the quality of the signal generated, if you change the external clock while waveform generation is in progress.

# NI PXI/PCI-5411/5431 (Video) Digital Pattern Connector

### (Video) Digital Pattern Connector

(VIDEO) DIGITAL PATTERN is a 16-bit digital I/O connector that contains the 16-bit digital pattern outputs, digital pattern clock output, marker output, external trigger input, and +5 V power output.

Refer to <u>SHC50-68 50-Pin Cable Connector</u> for information about adapting the connector from 50 to 68 pins.

### NI 5411/5431 DIGITAL PATTERN Pin Assignments

The following figure shows the NI 5411/5431 (VIDEO) DIGITAL PATTERN 50-pin VHDCI female connector.

	_				
	$ \subset $			,	
DGND	Ĺ	50	25		EXT_TRIG
NC		49	24		NC
DGND		48	23		NC
NC		47	22		NC
DGND		46	21		NC
NC		45	20		NC
DGND		44	19		NC
+5V		43	18		+5∨
DGND		42	17		+5∨
M AR KE R		41	16		+5∨
DGND		40	15		PCLK
RFU		39	14		RFU
DGND		38	13		RFU
RFU		37	12		RFU
DGND		36	11		PA(15)
P A(13)		35	10		PA(14)
DGND		34	9		PA(12)
P A(10)		33	8		PA(11)
DGND		32	7		PA(9)
PA(7)		31	6		PA(8)
DGND		30	5		PA(6)
PA(4)		29	4		PA(5)
DGND		28	3		PA(3)
PA(1)		27	2		PA(2)
DGND		26	1		PA(0)
		~	~		
			~~~	. 1	

The following table lists the pin names and signal descriptions used for the NI 5411/5431 (VIDEO) DIGITAL PATTERN connector.

Signal Name	Туре	Description
DGND		Digital ground.
EXT_TRIG	Input	External trigger—The external trigger input signal is a TTL-level signal that you can use to start or step through a waveform generation. Refer to <u>Triggering</u> for more information.
MARKER	Output	Marker—A marker is a TTL-level output signal that you can set up at any point in the waveform

		generating. You can use this signal to synchronize or trigger other devices at a certain time within waveform generation.
NC		Not connected.
PA<015>	Output	Digital pattern outputs—The 16-bit digital representation of the analog waveform is available on these output pins as digital pattern outputs along with the PCLK signal to which it is synchronized. This data is available directly from the memory after some Sample clocks pipeline delay. The digital pattern outputs are TTL output levels.
PCLK	Output	Digital pattern clock—The digital pattern clock output synchronizes the digital pattern output. This data is available directly from the memory after some Sample clocks pipeline delay. The PCLK output is a TTL output level.
RFU	<u> </u>	Reserved for future use. Do not connect signals to this pin.
+5V	Output	+5 V power—A +5 V output signal is available on the NI 5411/5431 to power external devices. The maximum current you can draw is 100 mA.

NI 5431 Exceptions				
Signal Name	Туре	Description		
PA<0>	Output	Vertical Sync (Vsync)k— The portion of the video signal that tells the display where to place the image in the top-to-bottom dimension.		
PA<1>	Output	Horizontal Sync (Hsync)k— The portion of the video signal that tells the display where to put the picture in the left-to-right dimension.		
PA<2>	Output	Composite Sync (Csync)k— Composite Synchronization signal; a single signal including both horizontal and vertical synchronization pulses.		

PA<3>	Output	Field Identification (Field ID)k— The field ID signal identifies the even or odd field in an interlaced video frame.
PA<415>	Output	Digital pattern outputs—The 12-bit digital representation of the analog waveform is available on these output pins as digital pattern outputs along with the PCLK signal to which it is synchronized. This data is available directly from the memory after some Sample clocks pipeline delay. The digital pattern outputs are TTL output levels.

SHC50-68 50-Pin Cable Connector

You can use an optional SHC50-68 50-pin-to-68-pin cable for pattern generation output. The cable connects to the NI PXI/PCI-5411/5431 (VIDEO) DIGITAL PATTERN VHDCI female connector.

Connecting the SHC50-68 Cable Connector

The following figure shows the 68-pin female connector pin assignments on the SHC50-68 cable.

			~	\sim	
]	
DGND	ĺ	50	25		EXT_TRIG
NC		49	24		NC
DGND		48	23		NC
NC		47	22		NC
DGND		46	21		NC
NC		45	20		NC
DGND		44	19		NC
+5V		43	18		+5∨
DGND		42	17		+5∨
M AR KE R		41	16		+5∨
DGND		40	15		PCLK
RFU		39	14		RFU
DGND		38	13		RFU
RFU		37	12		RFU
DGND		36	11		PA(15)
P A(13)		35	10		PA(14)
DGND		34	9		PA(12)
P A(10)		33	8		PA(11)
DGND		32	7		PA(9)
PA(7)		31	6		PA(8)
DGND		30	5		PA(6)
PA(4)		29	4		PA(5)
DGND		28	3		PA(3)
PA(1)		27	2		PA(2)
DGND		26	1		PA(0)
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			~~~	- 1	

### **Signal Descriptions**

The following table shows the pin names and signal descriptions used on the NI 5411/5431 (VIDEO) DIGITAL PATTERN connector.

Signal Name	Туре	Description
DGND		Digital ground.
EXT_TRIG	Input	External trigger—The external trigger input signal is a TTL-level signal that you can use to start or step through a waveform generation. Refer to <u>Triggering</u> for more information.
MARKER	Output	Marker—A marker is a TTL-level output signal that you can set up at any point in the waveform being generated. You can use this signal to synchronize or trigger other devices at a certain time within waveform generation.
NC		Not connected.
PA<015>	Output	Digital pattern outputs—The 16-bit digital representation of the analog waveform is available on these output pins as digital pattern outputs along with the PCLK signal to which it is synchronized. This data is available directly from the memory after some Sample clocks pipeline delay. The digital pattern outputs are TTL output levels.
PCLK	Output	Digital pattern clock—The digital pattern clock output synchronizes the digital pattern output. This data is available directly from the memory after some Sample clocks pipeline delay. The PCLK output is a TTL output level.
RFU		Reserved for future use. Do not connect signals to this pin.
+5V	Output	+5 V power—A +5 V output signal is available on the NI 5411/5431 to power external devices. The maximum current you can draw is 100 mA.

#### (VIDEO) DIGITAL PATTERN Connector Signal Descriptions

# NI 5411/5431 Digital Pattern Generation

The NI 5411/5431 has 16-bit digital pattern generation outputs at the <u>digital connector</u>. This digital data is first synchronized to the Sample clock and then buffered and sent to the connector through a 68  $\Omega$  series resistor. The Sample clock is also buffered and sent to the digital connector to latch the data externally. The following figure shows the data path for digital pattern generation.



*Output Enable

Because the digital pattern data does not go through the digital filter, the data is available directly from the memory. Direct memory access means a fixed delay of 26 Sample clocks between the analog waveform, which lags behind the digital waveform, and the digital patterns exists. Although you can disable the digital filter using the <u>niFgen Configure Digital Filter</u> VI or the <u>niFgen_DisableDigitalFilter</u> function in software, 26 Sample clock delay still exists.

You can enable or disable digital pattern generation by using the <u>niFgen</u> <u>Configure Digital Patterning</u> VI or the <u>niFgen_EnableDigitalPatterning</u> function. All <u>linking and looping</u> capabilities are available for digital pattern generation as well. If you select Function Generation mode, the function generation data appears at the digital I/O connector.

You can use digital pattern generation to test digital devices, such as serial and parallel DACs, and to emulate protocols.



**Note** At computer power-up and reset, digital pattern generation is disabled.

The following figure shows the timing waveforms for digital pattern generation;  $t_{clk}$  is the clock time period and  $t_{co}$  is the time delay from clock to output on pattern lines, such as PA<0..15>.



The Sample clock for integral subdivisions of 40 MHz always has a high pulse width of 25 ns. If the  $t_{co}$  time is insufficient for the hold time of the device, you can use the falling edge of the Sample clock output (PCLK) to register the digital pattern data.

### NI PXI/PCI-5411 SYNC Connector

The SYNC output is a TTL version of the sine waveform generated at the output. The SYNC output has a very high-frequency resolution, with a software-programmable clock source for many applications. You can also dynamically vary the duty cycle of the SYNC output between 20–80% by software control. The SYNC output derives from a comparator connected to the analog waveform and provides a meaningful waveform only when you generate a sine wave on the ARB output. The following figure shows the timing relationship between the SYNC and analog output waveform.



 $t_p$  is the time period of the sine wave generating and  $t_w$  is the pulse width of the SYNC output. The duty cycle is  $(t_w/t_p) \times 100\%$ .

## NI PXI/PCI-5411/5431 Power-Up and Reset Conditions

When you power up the computer, the NI 5411/5431 is in the following state:

- The output is disabled and set to 0 V.
- The Sample clock is set to 40 MHz.
- The trigger mode is set to Continuous.
- The trigger source is set to automatic (the software provides the triggers).
- The digital filter is enabled.
- Digital pattern generation is disabled.
- Output attenuation remains unchanged from its previous setting.
- The analog filter remains unchanged from its previous setting.
- Output impedance remains unchanged from its previous setting.

When you reset the device using NI-FGEN or another application software, the NI 5411/5431 is in the same state as shown at power up with the following differences:

- Output attenuation is set to 0 dB.
- The analog filter is enabled.
- Output impedance is set to 50  $\boldsymbol{\Omega}$
- The PLL reference frequency is set to 20 MHz (NI 5411 only).
- The PLL reference source is set to internal tuning (NI 5411 only).
- The RTSI clock source is disabled (NI 5411 for PCI only).
- The SYNC duty cycle is set to 50%.

# NI 5411 Theory of Operation

Expand this topic for information about the NI 5411 theory of operation.

### NI PXI/PCI-5411 Block Diagram

The following figure shows the NI PXI/PCI-5411 block diagram.



# NI PXI-5411/5431 Analog Output

Analog waveforms generate as follows:

- 1. The 12-bit digital waveform data is passed to a high-speed DAC.
- 2. A lowpass filter filters the DAC output.
- 3. This filtered signal is amplified before it goes to a 10 dB attenuator.
- Note You can fine tune the DAC output for gain and offset. Because the offset is adjusted before the main attenuators and amplifier, it is referred to as pre-attenuation offset. Separate DACs perform the fine tuning of gain and offset.
  - 4. The output from the 10 dB attenuator then goes to the main amplifier, which can provide up to  $\pm 5$  V levels into 50  $\Omega$ . An output relay can switch between ground level and the main amplifier.
  - 5. The output of this relay goes to a series of passive attenuators.
  - 6. The output of the attenuators goes through a selectable output impedance of 50  $\Omega$  or 75  $\Omega$  to the front panel connector.

The following figure shows the block diagram of analog waveform generation.



The following figure shows the timing relationships of the trigger input, waveform output, and marker output.  $t_{d1}$  is the pulse width on the trigger

signal.  $t_{d2}$  is the time delay from trigger to output on ARB output.  $t_{d3}$  is the time between the marker output and ARB output.  $t_{d4}$  is the pulse width on marker output.



Note You can switch off the analog lowpass filter at any time during waveform generation. When you change this setting, the bouncing of electromechanical relays on the NI PXI-5411/5431 distorts the output signal for about 10 ms.

## NI PXI/PCI-5411/5431 Pre-Attenuation Offset

The NI PXI/PCI-5411/5431 supports a DC offset of up to ±2.5 V before the attenuation chain. Unless the 10 dB attenuator is switched on, which occurs when the gain is less than 1.58 V or the amplitude is less then 3.16 V_{pk-pk}, the waveform maximum plus the offset must not exceed ±5 V into 50  $\Omega$  if it does, the waveform is clipped.

NI-FGEN automatically calculates the pre-attenuation offset value based on the DC offset and gain or amplitude values. In Arbitrary Waveform Generation mode (NI 5411/5431 only), the allowable DC offset range is dependent on the amplitude. For example, if you have a gain of 0.5 V or an amplitude of 1 V_{pk-pk}, the maximum DC offset you can apply is 0.25 V, which corresponds to a pre-attenuation offset of 2.5 V. In Function Generation mode, the allowable DC offset is independent of the amplitude.

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**Note** You can change the DC offset at any time during waveform generation.

## NI 5411/5431 Digital Filter Considerations

When you use external clocking, high-resolution clocking, or divide-by-n clocking, the actual update rate depends on the state of the digital filter.

For external clocking, if you enabled the digital filter, the actual update rate equals half the frequency of the external clock. In this case, the maximum frequency of the external clock is 40 MHz and the corresponding update rate achieved is 20 MHz. If you disabled the digital filter, the actual update rate equals the frequency of the external clock. In this case, the maximum frequency of the external clock is 40 MHz and the corresponding update rate equals the frequency of the external clock. In this case, the maximum frequency of the external clock is 40 MHz and the corresponding update rate achieved is also 40 MHz.

For high-resolution clocking, if you enabled the digital filter, the update rate is limited to 20 MHz. NI-FGEN reports an error if you disabled the digital filter specified an update rate greater than 20 MHz while high-resolution clocking is in use. If you disable the digital filter and high-resolution clocking is in use, the maximum update rate allowed is 40 MHz.

# NI PXI-5411/5431 External and High-Resolution Clocking

You can connect an external clock to the PLL Ref input connector of the NI PXI-5411/5431. To do this, you must set up the clock source in the software. Refer to the <u>Configure Reference Clock</u> and <u>Configure Clock</u> <u>Mode VIs or the niFgen_ConfigureRefClockSource</u> and <u>niFgen_ConfigureClockMode</u> functions for more information about setting up the clock. You can use an external clock as the Sample clock. The maximum frequency of the external clock is 40 MHz.

**Caution** You must not change the frequency of this clock during waveform generation (sweeping of external clock is not available). Changing the frequency of the clock during waveform generation can result in malfunctioning of the device. Change the clock frequency only before initiating the waveform generation. If any malfunction occurs, stop the waveform generation and reset the device to a known state before restarting.

NI PXI-5411/5431 signal generators also support an internal highresolution clocking mode. When you use this type of clock, you can set the Sample clock frequency to any value from 0–40 MHz with a resolution of approximately 40 MHz. This mode is useful for applications that require a precise clock source, which is not possible using the default counter-based clocking scheme. Use this clocking mode for applications such as CDMA, GSM, and ADSL waveform generation.

### NI PXI/PCI-5411/5431 Waveform Memory

NI PXI/PCI-5411/5431 signal generators use a waveform memory that is 16-bits wide. The standard memory size for the NI 5411 is 2,000,000 samples, and for the NI 5431 is 8,000,000 samples. With a minimum standard memory size of 2,000,000 samples, you can store very long waveforms on the device and obtain reliable waveform generation even at full speed. You can upgrade the NI 5411 to an 8,000,000-sample waveform memory by installing the 16 MB memory module. Refer to Installing the Optional Memory Module (NI 5411 only), for more information about the installation of the optional memory module.

As shown in the following figure, a 2,000,000-sample waveform memory is organized as eight banks of 256 k by 16-bit memory chips. An 8,000,000-sample waveform memory is organized as eight banks of 1 M by 16 bit memory chips. These eight banks are then shifted serially to achieve a single data stream of 16-bit words at 40 MHz.



## NI PXI/PCI-5411/5431 Waveform Generation

The NI 5411/5431 generates waveforms in two modes: <u>Arbitrary</u> <u>Waveform Generation</u> and <u>Function Generation</u>. Use Arbitrary Waveform Generation mode for any arbitrary waveform generation, and use Function Generation mode for standard frequency generation such as sine, TTL, square, and triangular waveforms.

Arbitrary Waveform Generation mode, which has more features and is more flexible than Function Generation mode, allows you to define waveforms as multiple waveforms. You can link and loop these waveforms in any order you want. Function Generation mode is better for generating standard waveforms that are repetitive in nature, such as sine, TTL, square, and triangular waveforms. Function Generation mode limits you to one waveform, and the waveform size must be exactly equal to 16,384 samples.

The following figure shows a block diagram of the data path for waveform generation.



The data for waveform generation can come from either the waveform memory module or DDS lookup memory, depending on the mode of waveform generation. This data is interpolated by a half-band digital filter and then fed to a high-speed DAC. The data has a pipeline delay of 26 Sample clocks through this digital filter. Although the digital filter can be disabled through software, there is still a 26 Sample clock delay. On the NI 5411/5431, the high-speed DAC is always updated at 80 MHz, but the maximum Sample clock for waveform memory is 40 MHz. The sample clock for the waveform memory can be further divided by a 16-bit counter. Therefore, the slowest sample rate is 40 MHz divided by 65,536, which is 610.35 Hz.



s **Note** For Function Generation mode, the actual sample rate of the DAC is always set at 40 MHz.

• NI 5431

When using the NI-Video application programming interface, to achieve a maximum update rate of exactly 40 MHz, you must set the video waveform type to PAL with the software. If the setting is NTSC, the maximum sample rate is not exactly 40 MHz. When programming with NI-FGEN, the maximum sample rate is exactly 40 MHz.

• NI PXI-5411/5431

You can use an external clock source as the Sample clock. To avoid device problems, do not change the frequency of this clock during waveform generation. Change the frequency only before initiating the waveform generation. If any malfunction occurs, stop the waveform generation and reset the device to a known state before restarting.

NI 5411/5431 signal generators also support an internal high-resolution clocking mode. When you use this type of clock, you can set the Sample clock frequency to any value from 0–40 MHz with a resolution of approximately 40 mHz. This mode is useful for applications that require a precise clock source that is impossible with the default counter-based clocking scheme.
## NI 5411/5431 Arbitrary Waveform Generation

The NI 5411 and NI 5431 are full-featured arbitrary waveform generators that you can use to create and generate any arbitrary waveform up to a sample rate of 40 MHz.



**Note** The NI 5411/5431 must have at least 256 samples in the waveform, and the waveform size should be a multiple of eight samples.

### NI PXI/PCI-5411/5431 Sample Size and Resolution

The NI 5411/5431 stores arbitrary waveforms in memory as 16-bit digital words. Only the 12 most significant bits are sent to the digital filter and the DAC.

## NI PXI/PCI-5411/5431 Minimum Waveform Size and Resolution

The memory architecture of the NI PXI/PCI-5411/5431 imposes certain requirements on the waveform size and resolution. The minimum waveform size for Arbitrary Waveform Generation mode is 256 samples, and the waveforms must be in multiples of eight samples. If these waveform requirements are not met, NI-FGEN returns an error. For example, if you request the NI 5411/5431 to load a waveform of 257 samples, NI-FGEN returns an error.

# NI PXI/PCI-5411/5431 Waveform Staging

The following figure shows waveform staging in hardware. The instruction FIFO contains the staging list, which the NI PXI/PCI-5411/5431 sequencer reads for waveform generation.



Instruction FIFO

Each stage is made up of four steps:

- Buffer number—Specifies the buffer number to generate.
- Buffer size—Specifies the total count of the buffer to generate. The total count may not be the actual size of the buffer. If the count is less than the actual size of the buffer, only a part of that buffer is used for that stage. If the count is more than the actual size of that buffer, part of the next sequential buffer is also used. If the buffer size is set to zero, the software automatically uses the true size of that buffer.
- Buffer loops—Specifies the number of times that the buffer loops. The maximum number of loops possible is 65,535.
- Marker offset—Specifies where the marker must generate within that buffer. For more information about markers, refer to <u>Marker</u> <u>Output Signal</u>.

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**Note** The maximum number of waveform stages the instruction FIFO can store for Arbitrary Waveform Generation mode is 292.

# NI PXI/PCI-5411/5431 Linking and Looping

You can load multiple waveforms in the memory of the NI PXI/PCI-5411/5431. A finite number of samples makes a waveform, also called a waveform segment. To generate these waveforms, prepare a staging list, or a sequence list, which contains a sequence of stages. Each stage specifies the waveform, its number of loops, and its marker offset.

The following figure shows the concepts of waveform samples, buffer/segment, stage, staging list, and linking and looping.



Waveform Sample A shows the concept of waveform samples used to create a waveform, shown in Waveform Buffer/Segment 1. In this example, Waveform Buffer/Segment 1 represents a single cycle of a sine wave, and the waveform samples in Sample A are 16-bit samples. Waveform Stage 1 shows a stage created from Buffer 1. Stage 1 is Buffer 1 with three cycle iterations.

Waveform Sample B shows samples for Waveform Buffer/Segment 2, which represents a triangular waveform. Waveform Stage 2 is created using two iterations of Buffer 2.

Waveform Stage 3 is created using a single iteration of Buffer 1.

These waveforms are linked in a sequence, as shown in the figure. The concept of using a staging list to generate waveforms is referred to as waveform linking and looping or waveform staging.

### NI 5411/5431 Markers

You can specify a marker by giving an offset count (in number of samples) from the start of the waveform specified by the stage. If the offset is out of range of the number of samples in that stage, the marker does not appear at the output. If the waveform loops multiple times in a stage, the marker generates the same number of times.

Note The marker begins generating on the last sample preceding the specified placement that is evenly divisible by eight and generates for eight Sample clocks. Therefore, the beginning of the marker is always within eight samples of the specified placement.

If you want a marker at an offset of zero from the start of the waveform, the marker is eight samples long beginning with the first sample. A marker at an offset of seven from the start of the waveform is also eight samples long beginning with the first sample, as shown in the following table. A marker at an offset of eight generates at positions 8–15.

Marker Requested from the Beginning of the Waveform	Marker Generated
At sample 0	Sample position 0–7
At sample 1	Sample position 0–7
At sample 7	Sample position 0–7
At sample 8	Sample position 8– 15
At sample 27	Sample position 24– 31
At sample 255	Sample position 248–255

#### **Generated Marker Positions**

The following figure shows an analog waveform generating at one connector and a marker generating at another I/O connector. Point A shows a marker generated for requested positions 0–7, and point B shows a marker generated for requested positions of 8–15.



#### Markers as Trigger Outputs

Note Marker output signals are an important feature for triggering other devices at a specified time while a waveform generation is in progress.

A delay of more than 76 Sample clocks from the external trigger (EXT_TRIG) edge to the analog waveform generation on the output connector exists. Therefore, synchronizing the NI 5411/5431 output signal to other devices with faster and more predictable trigger response times is difficult. For these applications, use the marker from the NI 5411/5431 as the trigger source for the other device. You can use the NI 5411/5431 marker over the RTSI bus, over the PXI trigger lines, or externally over the connector.

# NI PXI/PCI-5411/5431 Trigger

You can define the NI PXI/PCI-5411/5431 functionality by using the various trigger techniques described in this section.

The following list shows the types of trigger modes available:

Burst trigger mode

Continuous trigger mode

Single trigger mode

Stepped trigger mode

# NI PXI/PCI-5411/5431 RTSI/PXI Trigger Lines

### NI PCI-5411/5431

The NI PCI-5411/5431 contains seven trigger lines and one RTSI clock line available over the RTSI bus to send and receive NI PCI-5411/5431-specific information to other devices that have RTSI connectors.

The following figure shows the RTSI trigger lines and routing of NI PCI-5411/5431 for signals to the RTSI switch.



For phase locking to other devices as a master, the NI PCI-5411 sends an onboard 20 MHz signal to the RTSI Osc line as a device clock signal. For locking to other devices as a slave, the NI PCI-5411 receives the RTSI Osc line as an RTSI clock signal.



**Note** Phase locking multiple NI 5431 signal generators is not supported when generating video waveforms.

### NI PXI-5411/5431

The NI PXI-5411/5431 can receive a hardware trigger from another device as an RTSI trigger signal on any of the RTSI/PXI trigger lines.

The following figure shows the PXI trigger lines and routing of NI PXI-5411/5431 signals to the RTSI switch.



You can also route NI PXI-5411/5431 signals as follows:

- Route the marker generated during waveform generation in Arbitrary Waveform Generation mode to any of the RTSI/PXI bus trigger lines.
- Route the Start trigger signal generated on the NI PXI-5411/5431 to other devices through any of the RTSI/PXI bus trigger lines.
- Route the SYNC output generated on the NI PXI-5411/5431 to other devices through any of the RTSI/PXI bus trigger lines. You can use this signal to give other devices an accurate and fine frequency resolution clock.

For phase locking to other devices, the NI PXI-5411 receives the PXI backplane 10 MHz Osc as a Reference clock signal. All the NI PXI-5411 signal generators use this common signal as the Reference clock for phase locking.

The bi-directional device SYNC signal is used as a trigger signal to synchronize multiple devices only during a <u>master/slave operation</u>. For general-purpose triggering, you must use either a Start trigger for the outgoing trigger or a RTSI trigger for the incoming trigger.



**Note** Phase locking multiple NI 5431 devices is not supported when generating video waveforms.

## NI PXI/PCI-5411/5431 Trigger Modes

NI PXI/PCI-5411/5431 signal generators have four trigger modes: <u>Single</u>, <u>Continuous</u>, <u>Stepped</u>, and <u>Burst</u>. These trigger modes are available for both Arbitrary Function Generation and Direct Digital Synthesis modes.

## NI PXI/PCI-5411/5431 Stepped Trigger Mode

After a Start trigger is received, the waveform defined by the first stage generates. Then, the device waits for the next trigger signal. On the next trigger, the waveform described by the second stage generates, and so on. After the staging list completes, the waveform generation returns to the first stage and continues in a cyclic fashion.

You can use the Stepped Trigger mode with both the Arbitrary Waveform Generation and Function Generation modes of waveform generation as follows:

• Arbitrary Waveform Generation mode—The following figure uses the stages to show a Stepped trigger mode of operation for the Arbitrary Waveform Generation mode. If a trigger is received while a stage is generating, the trigger is ignored. A trigger is recognized only after the stage has completely generated.



*The first eight samples of the next stage are generated repeatedly.

After any stage generates, the first eight samples of the next stage repeat continuously until the next trigger is received.



**Note** For Stepped trigger mode, you can pre-define the state in which a stage ends by making the first eight samples of the next stage represent the state you want to settle.

• Function Generation mode—When using the Function Generation mode of waveform generation, Stepped trigger mode operates the same as <u>Burst trigger mode</u>.

## NI PXI/PCI-5411/5431 Burst Trigger Mode

After receiving a Start trigger, the waveform defined by the first stage generates until receiving another trigger. At the next trigger, the waveform of the previous stage completes before the waveform defined by the second stage generates. After the staging list completes, the waveform generation returns to the first stage and continues in a cyclic fashion.

You can use Burst trigger mode with both the Arbitrary Waveform Generation and Function Generation modes as follows:

• Arbitrary Waveform Generation mode—The following figure shows a Burst trigger mode of operation for Arbitrary Waveform Generation mode using the stages shown. In this mode, the loop information associated with each stage is not used. The trigger causes the generation to proceed to the next stage after the previous waveform completes.



• **Function Generation mode**—The following figure shows a Burst trigger mode of operation for Function Generation mode. Switching from stage to stage is phase continuous. In this mode, the time instruction is not used. The trigger paces the waveform generation from one frequency to the other.



## NI PXI/PCI-5411/5431 Master/Slave Operation

You can phase lock the NI 5411 to other devices or other NI 5411 signal generators in two different ways to synchronize multiple devices in a test system.

• NI PCI-5411/5431

The following figure shows master/slave configurations for phase locking any NI signal generator with RTSI bus capability as the master.



To phase lock an NI 5411/5431 to this master, complete the following steps:

- 1. Set the NI master device to send a 20 MHz signal over the RTSI bus on the RTSI Osc line. If this device is an NI 5411/5431, set the source for the RTSI clock line to device_clock for NI-FGEN and internal for LabVIEW.
- 2. Set up the slave devices so that the RTSI clock line is the PLL reference source.
- 3. Set the PLL reference frequency parameter to 20 MHz. The devices are now frequency locked to the master.
- 4. To further phase lock the devices, set up the master to send the trigger signal on one of the RTSI trigger lines.
- 5. Set up the slave devices to receive their trigger signal on the RTSI bus.
- 6. Start the waveform generation on all the slaves.
- 7. Start the waveform generation on the master.

The master triggers all the slaves that are phase and frequency locked to each other and the master.

The following figure shows the master/slave configuration for phase locking an external device as the master.



External Master Configuration

To phase lock NI 5411 signal generators to this master, complete the following steps:

- 1. Set the master device to send any valid Reference clock to the PLL reference input connector.
- 2. Set up the slave devices with the I/O connector as the PLL reference source.
- 3. Set the PLL reference frequency parameter to the clock frequency sent by the master. The devices are now frequency locked to the master.
- 4. To further phase lock the devices, connect the trigger source to the trigger input of the 50-pin digital connectors of all the devices, and set up the slaves to receive the triggers on trigger input connector.
- 5. Start the waveform generation on all the slaves.
- 6. Activate the external trigger signal. All the slaves are triggered at the same time and are phase and frequency locked.

#### • NI PXI-5411/5431

To phase lock NI PXI-5411/5431 signal generators, complete the following steps:

- 1. Set all the NI 5411/5431 signal generators to accept the 10 MHz Osc line on the PXI backplane as the PLL Reference clock signal.
- 2. Set the PLL reference frequency to 10 MHz. The devices are now frequency locked to the backplane 10 MHz Osc line.
- 3. Select the Sample clock source to internal divide-down mode, high-resolution mode, or external clocking mode. External clocking mode results in the best synchronization.
- 4. To further phase lock the devices, set up the master to send the

trigger signal on one of the PXI trigger lines.

- 5. Set up the slaves to receive their trigger signal on the PXI trigger bus.
- 6. Set up the master to send the device_SYNC signal on the PXI trigger line and the slaves to receive the device_SYNC signal on the same PXI trigger line.
- 7. Start the waveform generation on all the slaves.
- 8. Start the waveform generation on the master.

The master triggers all the slaves, which are phase and frequency locked to each other and the master.

Note If two or more NI 5411 signal generators are running in Direct Digital Synthesis mode and are locked to each other using the same Reference clock, they are frequency locked, but the phase relationship is indeterminate.

### • NI PCI-5431 Video Generation

Note When generating a video waveform, do not phase lock the NI 5431 if the Video Waveform Type property or the <u>NIFGEN_ATTR_VIDEO_WAVEFORM-TYPE</u> attribute is used to set the internal frequency of the device. For synchronized video generation, a master NI 5431, which is run with the Video Waveform Type property or the NIFGEN_ATTR_VIDEO_WAVEFORM_TYPE attribute set, provides a reference 20 MHz signal over the RTSI bus. The slaves run with the Video Waveform Type property or the NIFGEN_ATTR_VIDEO_WAVEFORM_TYPE attribute *not* set, phase locking to the external 20 MHz reference, thereby running at the correct clocking frequency.

The following figure for master/slave configurations for phase locking shows an NI PCI-5431 as the master.



RTSI Bus Master/Slave Configuration Device To phase lock an NI PCI-5431 to this master, perform the following steps:

- Set the NI 5431 (master) to send a 20 MHz signal over the RTSI bus on the RTSI Osc line. Set the source for the RTSI clock line to device_clock for NI-FGEN and internal for LabVIEW. Set the Video Waveform Type property or the NIFGEN_ATTR_VIDEO_WAVEFORM_TYPE attribute that is generating.
- 2. Set up the slave devices so that the RTSI clock line is the PLL Reference source. Ensure that Video Waveform Type property or the NIFGEN_ATTR_VIDEO_WAVEFORM_TYPE attribute is not being set.
  - Note The Video Waveform Type property is set in the NI 5431 HL Setup Attributes VI. Remove this property node for all slave devices.
- 3. Set the PLL reference frequency parameter to 20 MHz. The devices are now frequency locked to the master.
- 4. To further phase lock the devices, set up the master to send the trigger signal on one of the RTSI trigger lines.
- 5. Set up the slave devices to receive the trigger signal on the RTSI bus.
- 6. Start the waveform generation on all the slaves.
- 7. Start the waveform generation on the master.

The master triggers all the slaves that are phase and frequency locked to each other and the master.

### • NI PXI-5431 Video Generation

The NI PXI-5431 does not support synchronization through phase locking when the Video Waveform Type property or the

NIFGEN_ATTR_VIDEO_WAVEFORM_TYPE attribute is set. However, PAL video generation is still possible by clocking the NI 5431 normally. To do generation or clocking, remove the property node that sets the Video Waveform Type in the NI 5431 HL Setup Attributes VI.



**Note** If two or more NI 5411/5431 signal generators are running in Arbitrary Waveform Generation mode and are locked to each other using the same Reference clock, you see a maximum phase difference of one Sample clock on the locked devices when they are triggered at the same time.

## NI PXI/PCI-5411/5431 Specifications

For information about the NI PXI/PCI-5411/5431 specifications, refer to the <u>NI PXI/PCI-5411/5431 Specifications</u>. You can access these specifications by navigating to **Start»All Programs»National Instruments»NI-FGEN»Documentation»Hardware Specifications**, or you can visit <u>ni.com/manuals</u>.

### NI PXI/PCI-5411 Calibration

Before shipping you the NI PXI/PCI-5411, NI calibrated your device to ensure that all features are within specifications.

Calibration is a set of operations that compares the values indicated by a measuring instrument or measuring system to the corresponding values realized by external standards. The result of calibration can be used to determine the measurement error and can correct for it in the adjustment process.

The calibration process consists of verifying, adjusting, and reverifying a device. During verification, you compare the measured performance to an external standard of known measurement uncertainty to confirm that the product meets or exceeds specifications. During adjustment, you correct the measurement error of the device by adjusting the calibration constants and storing the new calibration constants in the EEPROM. The host computer reads the calibration constants and the software uses them to compensate for errors in the data and to present calibrated data to the user.

For more information about calibrating NI signal generators, refer to <u>ni.com/calibration</u>.

# NI 5411/5431 Accessories

National Instruments offers a variety of products to use with NI 5411/5431, including probes, cables, and other accessories, such as:

- Shielded and unshielded I/O connector blocks (SCB-68, TBX-68, CB-68)
- 16 MB memory module (optional)
- RTSI bus cables

The following table lists recommended part numbers for cables that you can use with NI 5411/5431 signal generators.

Product	Cable Name	Part Number	Cable Description
AT and PCI-5411	SMB 110	763405- 01	50 $\Omega$ SMB male to BNC male, 1 m coaxial cable
	SMB 300	763388- 01	50 $\Omega$ SMB male to alligator clip, 1 m cable
	SHC50- 68 (0.5 m)	184748- 0R5	Shielded 50-pin male VHDSCSI to 68-pin female SCSI 1 m cable (also available in 0.5 m and 2 m lengths)
	SHC50- 68 (1 m)	184748- 01	
	SHC50- 68 (2 m)	184748- 02	
	RTSI Bus Cables		Ribbon cables for connecting timing and synchronization signals among Measurement, Vision, Motion, and CAN devices.
	2 devices 776 02	776249- 02	
	3 devices	776249- 03	
	4 devices	776249- 04	
	5 devices	776249-	

		05	
	Extended RTSI	777562- 05	
PXI- 5411/5431	SMB 110	763405- 01	50 $\Omega$ SMB male to BNC male, 1 m coaxial cable
	SMB 111	763422- 0	75 $\Omega$ SMB male to BNC male, 1 m coaxial cable
	SMB 300	763388- 01	50 $\Omega$ SMB male to alligator clip, 1 m cable
	SHC50- 68 (0.5 m)	184748- 0R5	Shielded 50-pin male VHDSCSI to 68-pin female SCSI 1 m cable (also available in 0.5 m and 2 m lengths)
	SHC50- 68 (1 m)	184748- 01	
	SHC50- 68 (2 m)	184748- 02	
	IMAQ- BNC-1	18388 <mark>2-</mark> 02	BNC-to-BNC Analog Camera Cable (Video), 2 m (RG-59)

### National Instruments Connector Blocks

Product	Part Number	Description
SCB-68	776844- 01	Shielded I/O connector block for connection to cables with 68-pin connectors.
CA- 1000	777664- 01	Shielded enclosure for signal conditioning
TBX-68	777141- 01	I/O Connector Block with DIN Rail Mounting
CB- 68LP	777145- 01	Low-cost accessory with 68 screw terminals for easily connecting to 68-pin DAQ devices.
CB- 68LPR	777145- 02	Low-cost accessory with 68 screw terminals for easily connecting to 68-pin DAQ devices.

### Third Party Vendor Optional Cable Accessories

Product	Part Number	Vendor	Cable Type
NI 5411/5431	BNC-C- xx	ITT Pomona Electronics	BNC male to BNC male, 50 $\Omega$ cable
	2249-E- xx		BNC male to BNC male, 75 $\Omega$ cable
	5319		BNC female to RCA phono plug adapter
	4119-50		BNC 50 Ω feed-through terminator adapter
	3283		BNC female-female adapter

For more information about these products, visit <u>ni.com</u>.

# NI PXI/PCI-5411 Installing the Optional Memory Module

The standard onboard memory for the NI PXI/PCI-5411 is 4 MB. You can upgrade to a 16 MB memory module to store large waveforms directly on the card. Perform the following steps to install the new memory module:

- 1. Turn off the computer and remove the top cover or access port to the I/O channel.
- 2. Unscrew the bracket and remove the NI 5411 from the slot it has been plugged into.
- 3. Gently place the NI 5411 on a flat surface with the component and memory module side facing up.
- 4. Unfasten the two screws on the side of the memory module.
- 5. Gently unplug the memory module from the main module and store the old memory module in an antistatic bag to avoid damage to the components.
- 6. Properly align the new 16 MB memory module over the connectors and plug it into the connectors.
- 7. Fasten the two screws you removed in step 4.
- 8. Follow the regular installation steps described in <u>NI Signal</u> <u>Generators Getting Started Guide</u>.

# NI 5412 Overview

The NI 5412 is a 100 MS/s, 14-bit arbitrary waveform generator with the following features:

- One 14-bit resolution output channel
- Output amplitude up to 12  $V_{pk\text{-}pk}$  into a 50  $\Omega$  load
- Offset up to ±25% of V_{pk-pk}
- Up to 20 MHz sine output
- Up to 5 MHz square
- Up to 1 MHz triangle, ramp-up, and ramp-down
- Software-selectable output impedances (50  $\Omega$  or 75  $\Omega)$  and output attenuation levels from 0 dB to 51 dB
- High-Resolution, Divide by N, and external clocking
- PLL synchronization to external clocks or to PXI_CLK10
- NI-TClk support for multi-module synchronization. Refer to Start»All Programs»National Instruments»NI-TClk for more information.
- Sampling rate up to 100 MS/s
- Up to 256 MB of onboard waveform memory
- Waveform linking and looping for arbitrary waveform generation
- Digital filters
- Digital gain
- Two external trigger inputs
- Marker as trigger output
- PXI trigger/RTSI lines

All NI 5412 devices follow industry-standard Plug and Play specifications for the PXI bus, and offer seamless integration with compliant systems.

# NI PXI-5412/5421/5422/5441 Front Panel

The following figure shows the NI PXI-5412/5421/5422/5441 front panel. This front panel has four SMB connectors and an optional 68-pin male VHDCI connector. The male VHDCI (Digital Data & Control) connector is not available on the NI 5412 or the NI 5421/5422 with the 8 MB memory option.



The  $\underline{CH 0}$  SMB connector is the analog output from which arbitrary waveforms are generated.

The <u>CLK IN</u> SMB connector provides the device with an external reference or external Sample clock.

The <u>PFI 0 and PFI 1</u> SMB connectors are multi-directional connections for a number of different signals.

DIGITAL DATA & CONTROL is an optional 68-pin male VHDCI connector that contains the 16-bit LVDS digital pattern outputs.

## NI 5412/5421/5422/5441 CH 0 Connector

The CH 0 connector provides the analog waveform output. The maximum output levels from this connector depend on the type of load termination. If the output of the module terminates into a 50  $\Omega$  load, the maximum output levels are ±6 V as shown in the following figure.



If the output of the module terminates into a high-impedance load (HiZ), the maximum output levels are  $\pm 12$  V. If the output terminates into any other load, the levels are as follows:

 $V_{out} = \pm [R_L / (R_L + R_O)] \times 12 V$ 

**Note** For loads less than 50  $\Omega$ , load impedance compensation only supports combinations of a gain and load impedance that meet the previous V_{out} equation.

where

Vout is the maximum peak output voltage level

 $R_L$  is the load impedance in ohms

 $R_O$  is the output impedance of the module

By default,  $R_O = 50 \Omega$ , but you can set the output impedance to 75  $\Omega$  in NI-FGEN. Refer to the <u>niFgen Configure Output Impedance</u> VI or <u>niFgen_ConfigureOutputImpedance</u> function for more information about configuring the output impedance.

You can set the amplitude of the generated output signal in terms of peak voltage by setting the gain value. NI-FGEN calculates and sets the correct amount of attenuation required for the desired gain value. Refer to the <u>Arbitrary Waveform Gain</u> or <u>Amplitude</u> properties, or the <u>NIFGEN_ATTR_ARB_GAIN</u> or the <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u>

attribute for more information about configuring the output signal amplitude.

### Load Impedance Compensation

The NI 5412/5421/5422/5441 has the ability to configure the output signal amplitude based on a user-configured load-impedance setting. This is desirable for using the NI 5412/5421/5422/5441 with loads that have between 0  $\Omega$  and a high impedance. Refer to the <u>module specifications</u> for information about the output impedance tolerance.

By default, NI-FGEN assumes that the load impedance is equal to the output impedance. If they do not match, you have the option to change the load impedance value that NI-FGEN uses in its load-impedance compensation algorithm. NI-FGEN takes the load impedance into account for setting the amplitude, and provides the amplitude specified in the configured gain setting, eliminating the need to use the voltage divider equation. NI-FGEN compensates to give the desired peak-to-peak voltage amplitude or arbitrary gain (relative to 1 V). Refer to the Load Impedance property or the NIFGEN ATTR LOAD IMPEDANCE attribute for more information about load impedance.

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**Note** The voltage output levels are set in the software and are based upon a 50  $\Omega$  load termination by default, or based on the load resistance as specified by the user.

For specifications about the waveform output signal, refer to the <u>module</u> <u>specifications</u>.

### NI 5412/5421/5422/5441/5442 **CLK IN Connector**

The CLK IN front panel connector can accept an external Reference clock or external Sample clock.



**Caution** Do *not* change the external clocks while generating waveforms. Only modify the frequency of the external clock before you start the waveform generation or *after* you stop the waveform generation. NI cannot guarantee the quality of the generated signal if you change the external clock during waveform generation.
## **External Reference Clock Input**

The CLK IN connector can accept a Reference clock from an external source and phase lock the internal clock of the signal generator to this external Reference clock. Refer to the <u>device specifications</u> for the allowable Reference clock frequencies and signal characteristics.

The Reference clock uses the internal clock by default. Refer to the niFgen Configure Reference Clock VI or the niFgen_ConfigureReferenceClock function for more information about configuring the Reference clock source.

When configuring an external Reference clock, you must configure the external Reference clock frequency if it is different from the 10 MHz default setting. Refer to the <u>niFgen Configure Reference Clock</u> VI or the <u>niFgen ConfigureReferenceClock</u> function for more information about configuring the Reference clock frequency.

Note You also can phase–lock the signal generator to other NI devices using the common PXI 10 MHz backplane clock on PXI devices or the RTSI 7 line on PCI devices. Refer to <u>PLL Reference</u> <u>Sources</u> for more information about configuring the Reference clock.

## **External Sample Clock Input**

In addition to phase-locking, the CLK IN connector also can receive an external Sample clock. Refer to the device specifications for the allowable external Sample clock frequencies and signal characteristics.



**Caution** When configuring an external Sample clock, set the sample rate to the exact frequency you are using to avoid data errors. Refer to the niFgen Set Sample Rate VI or niFgen ConfigureSampleRate function for more information about setting the sample rate.

You can configure the Sample clock source with niFgen Configure Sample Clock Source VI or the niFgen ConfigureSampleClockSource function. The Sample clock uses the internal clock by default.

# NI 5412/5421/5422/5441/5442 **PFI Connectors**

PFI 0 and PFI 1 are bidirectional connectors. As an input, the PFI terminals can accept a trigger from an external source that can start or step through waveform generation.

As an output, the PFI lines can route a signal out from the following sources:

- Marker events
- Start trigger
- PLL Reference clock source
- Sample Clock Out (with /K where K is an integer used to divide the Sample clock)
- Script trigger (not available on the NI 5412)
- Started, Done, and Ready for Start events
- Sample clock timebase (with /N where N is an integer used to divide the Sample clock timebase frequency)

Refer to the device specifications for information about acceptable input signal characteristics for the PFI lines, as well as the output signal characteristics.

🕅 Note PFI 0 driver circuitry has been optimized to have lower jitter than PFI 1 for exporting the Sample clock or the PLL Reference clock source.

# NI PXI-5412 Block Diagram

This topic contains information about the NI PXI-5412 top-level block diagram and descriptions of the individual blocks.



### Legend

Note If it is installed in any slot other than Slot 2 of the PXI chassis, the NI 5412 can receive a signal on the PXI_STAR line and can route a signal on the PXI_STAR line back to Slot 2 of the PXI chassis.

The following list describes the individual blocks:

- Onboard Memory stores the waveform data and generation instructions that you load into the device.
- *Clocking* allows you to create your Sample clock and Reference clock.
- The Waveform Generation Engine retrieves the waveform data and instructions from the Onboard Memory using the Sample clock. The Waveform Generation Engine also uses this clock to retrieve

triggers from *Trigger and Event Control*.

- The output from the *Waveform Generation Engine* is sent to the *DAC* device after any digital gain is applied.
- The *DAC* also contains a selectable *Digital Filter*, which interpolates and filters the waveform data.
- The waveform data is sent from the *DAC* to the *Analog Output path* where the waveform data is amplified.
- The *Routing Matrix* allows flexible routing of the PXI Trigger lines (RTSI) and the external PFI lines.

# NI 5412 Analog Output

The following figure shows the NI 5412 Analog Output signal path.



### Legend

NI 5412 Analog waveforms are generated as follows:

- 1. The 14-bit digital waveform data from the Waveform Generation Engine is passed to a to a digital gain circuit then a high-speed DAC. This DAC also implements a portion of the Analog Output signal path attenuation with a range of 0 dB to 3 dB. Refer to the module specifications for the exact resolution. You can adjust the amount of attenuation by configuring the <u>Arbitrary Waveform Gain</u> or <u>Amplitude</u> properties, or the <u>NIFGEN_ATTR_ARB_GAIN</u> or <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u> attributes. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting.
- 2. Following the DAC are the High-Gain and Low-Gain amplifiers.

NI-FGEN selects the High-Gain or Low-Gain Amplifier paths by default. To select the path manually, refer to the <u>Analog Path</u> property or <u>NIFGEN_ATTR_ANALOG_PATH</u> attribute.

- 3. The signal then passes through attenuators, and amplifiers.
- 4. The signal then passes through the DC Offset Amplifier that adds the desired DC offset voltage. You can adjust the amount of DC offset added to the signal, up to one half the value of the NI-FGEN gain setting. For more information, refer to the <u>Arbitrary Waveform</u> <u>Offset</u> and <u>DC Offset</u> properties, or the <u>NIFGEN_ATTR_ARB_OFFSET</u> and <u>NIFGEN_ATTR_FUNC_DC_OFFSET</u> attributes.
- 5. The signal then passes through the Pre-Amp Attenuation section, a set of selectable solid-state attenuators that provide 0 dB to 12 dB of attenuation in 3 dB increments. You can adjust the amount of attenuation by adjusting NIFGEN_ATTR_ARB_GAIN. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting. Refer to the <u>Arbitrary Waveform</u> <u>Gain</u> and <u>Amplitude</u> properties, or the <u>NIFGEN_ATTR_ARB_GAIN</u> and <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u> attributes for more information.
- 6. Following the Pre-Amp Attenuation section, the signal can take one of two paths: the High-Gain or Low-Gain Amplifier path. NI-FGEN automatically selects the best amplifier path between the High-Gain and Low-Gain amplifiers by default based on the gain or amplitude setting. Alternatively, you can set the signal path to remain constant regardless of the gain setting for applications requiring one path or the other. Refer to the <u>Analog Path</u> property or the <u>NIFGEN_ATTR_ANALOG_PATH</u> attribute for more information.
  - a. The High-Gain Amplifier path is used for waveform output voltages greater than  $\pm 1.0$  V into 50  $\Omega$ . The amplifier has a fixed gain and is included in the signal path to enable the AWG to provide the maximum V_{pk-pk}.
  - b. The Low-Gain Amplifier path is used for waveforms that have all output voltages equal to or smaller than  $\pm 1.0$  V into 50  $\Omega$ . The amplifier has a fixed gain.
- 7. The signal passes through the Post Amp Attenuation section, a

set of two passive attenuators 12 dB and 24 dB. You can adjust the amount of attenuation by configuring the <u>Arbitrary Waveform</u> <u>Gain</u> and <u>Amplitude</u> properties, or the <u>NIFGEN_ATTR_ARB_GAIN</u> and <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u> attributes. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting.

- 8. The signal then passes through the Output Enable relay. When the Output Enable relay is disabled, ground is connected to the output through a 50  $\Omega$  or a 75  $\Omega$  resistor. Intentionally, waveform generation continues while the output enable relay is disabled. When the relay is enabled, the analog waveform is seen at the CH 0 connector. You can enable or disable the output of the analog waveform generator, refer to the <u>niFgen Output Enable</u> VI or the <u>niFgen_ConfigureOutputEnabled</u> function for more information.
- The signal then passes through a 50 Ω/75 Ω selector to the CH 0 connector. You can configure the output impedance of the analog waveform generator, refer to <u>niFgen Configure Output</u> <u>Impedance</u> VI or the <u>niFgen_ConfigureOutputImpedance</u> function.
- Note The NI 5412 uses mechanical relays to switch between the optional paths and sections in the Analog Out path. When you change a setting that results in a relay to switch, the bouncing of electromechanical relays on the NI 5412 distorts the output signal for about 10 ms.

# NI 5412 Waveform Amplitude Control

The NI 5412 uses both amplifiers and attenuators to achieve needed amplitude settings.

## **Output Paths and Amplifiers**

The following figure shows two different gain paths: the High-Gain Amplifier path and the Low-Gain Amplifier path.

The Low-Gain Amplifier path has a 2 V_{pk-pk} amplifier and is used for waveforms that have all output voltages equal to or smaller than 2.0 V_{pk-pk} into matched load impedance. The High-Gain Amplifier path has a 12 V_{pk-pk} amplifier and is used for waveforms that have output voltages greater than 2.0 V_{pk-pk} into matched load impedance. The gains of the amplifiers are constant. NI-FGEN automatically selects by default between the high-gain and low-gain amplifiers, depending on the NI-FGEN gain setting. Refer to the <u>Arbitrary Waveform Gain</u> or <u>Amplitude</u> properties, or the <u>NIFGEN ATTR ARB GAIN</u> or <u>NIFGEN ATTR FUNC AMPLITUDE</u> attributes for more information.

You can configure the High-Gain or the Low-Gain Amplifiers to remain in the Analog Output path regardless of gain setting. Refer to the <u>Analog</u> <u>Path</u> property or the <u>NIFGEN_ATTR_ANALOG_PATH</u> attribute for more information. Configuring the Low-Gain Amplifier path to remain constant regardless of the gain setting affects the maximum output value allowable for that particular gain setting. The maximum gain setting for an Analog Output path configured to Low-Gain Amplifier path is 1.0. The maximum allowable gain setting with NI-FGEN automatically selecting the Gain Amplifier path is 6.0. Gain is a unitless value.

In addition, the DC Offset Amplifier for adding <u>DC offset</u> to the signal is in the High-Gain and Low-Gain Amplifier paths prior to the attenuators and amplifiers. The DC Offset Amplifier can be fine-tuned for adding offset to your signal. This fine-tuning of the main DC Offset Amplifier is performed by the Offset DAC.

## NI 5412 Attenuation

The Analog Output signal path has two passive attenuation sections. Pre-Amp Attenuation is prior to the High-Gain and Low-Gain Amplifier paths, and Post-Amp Attenuation is after the High-Gain and Low-Gain Amplifier paths. In addition, the main DAC provides 0 dB to 3 dB of signal attenuation. The amplitude control is implemented after the DAC. Attenuating the DAC output signal allows you to vary your signal amplitude and still maintain the dynamic range of the DAC. You do not lose any bits from the digital representation of the signal as does the method of controlling amplitude by using smaller data ranges of the DAC, sacrificing dynamic range.

For the Low-Gain Amplifier and the High-Gain Amplifier paths, maximum attenuation is 51 dB. NI-FGEN automatically determines the correct value of attenuation in dB, and configures the attenuation based on the set gain. The minimum gain setting for an Analog Output path configured to High-Gain Amplifier path is .01691. The minimum allowable gain setting with NI-FGEN automatically selecting the Low-Gain Amplifier path is .00282. Gain is a unitless value.

NI-FGEN calculates and sets the correct amount of attenuation required that corresponds to your NI-FGEN gain setting. The correct amount of attenuation is implemented in the Pre-Amp and Post-Amp Attenuation sections to best achieve the desired output signal amplitude. You can set the amount of gain with the <u>Arbitrary Waveform Gain</u> property or the <u>NIFGEN_ATTR_ARB_GAIN</u> attribute.

### **Pre-Amp Attenuation**

The Pre-Amp Attenuation section is before the Low-Gain and High-Gain amplifiers. The attenuators provide a range of attenuation from 0 dB to a maximum of 12 dB in steps of 3 dB. NI-FGEN automatically controls the value of attenuation set in the Pre-Amp Attenuation section depending on the set gain.

Pre-Amp Attenuation improves the distortion of a signal because amplifiers provide lower distortion performance with smaller signals. However, attenuation lowers the amplitude of both the signal and the noise in a signal as the signal-to-noise ratio is unchanged upon attenuation. Amplifiers also have a fixed noise associated with them. The total noise at the amplifier output is obtained by taking the root of the sum of squares of the following factors:

- The input signal noise multiplied by the gain of the amplifier
- The amplifier noise

The total noise is dominated by the larger factor. If the signal is attenuated so that its noise when multiplied by gain at the amplifier input is smaller than the amplifier noise, then the output has a higher signal-tonoise ratio. This is a good reason to implement some of the AWG overall attenuation as Pre-Amp attenuation.

### **Post-Amp Attenuation**

The Post-Amp Attenuation section is after the High-Gain and Low-Gain Amplifiers. The attenuators provide a range of attenuation from 0 dB to a maximum of 36 dB in steps of 12 dB. NI-FGEN automatically controls the value of attenuation set in the Post-Amp Attenuation section dependent on the set gain.

### **DAC** Attenuation

The main DAC output can be fine-tuned for attenuation, which provides 0 dB to 3 dB of the Analog Output path signal attenuation. This fine-tuning of the main DAC attenuation is performed by the Gain DAC. The main DAC also provides the fine resolution for the attenuation settings.

### **Summary of Gain Settings**

The following table summarizes the maximum and minimum gain setting that you can apply for the three NI-FGEN Analog path options. The default path is automatic. NI-FGEN automatically sets the path and correct amount of attenuation depending on the configured gain setting. These values assume a matched load impedance. Refer to the module specifications for more information about gain resolution.

NI 5412 Analog Path Gain Summary (matched load impedance)			
NI-FGEN Analog Path	Maximum Gain Value	Minimum Gain Value	
Automatic (default)	6.000	2.817 m	
Fixed Low-Gain Amplifier	1.027	2.817 m	
Fixed High-Gain Amplifier	6.000	16.91 m	
Note: Gain is unitless.			

# NI 5412/5421/5422/5441 DC Offset

The NI 5412/5421/5422/5441 supports a DC offset before the attenuation chain that affects the maximum value of DC offset that is possible for a given gain setting. This pre-attenuation architecture requires two rules for setting the DC offset:

- 1. The magnitude of the maximum value of offset can be no more than ½ of the configured gain setting for the NI 5412/5421/5441 and no more than the gain setting for the NI 5422.
- 2. The waveform maximum plus the offset must not exceed  $\pm 6$  V into 50  $\Omega$ ; if it does, the waveform is clipped.

For example, if you have set a gain of 5, which corresponds to an amplitude of 5 V, and the waveform is a sine wave using the full range of the DAC, the maximum DC offset you can apply with out clipping the sine wave is  $\pm 1$  V. At this point, output voltages of the sine waveform have reached the maximum amplitude that the device supports. If you increase the DC offset further, the top portion of the waveform at 6 V will be clipped.

NI-FGEN automatically calculates the pre-attenuation offset value based on the set DC offset and gain values. You can change the DC offset at any time during waveform generation. Refer to the <u>Arbitrary Waveform</u> <u>Offset</u> property or the <u>NIFGEN_ATTR_ARB_OFFSET</u> attribute for more information about setting the DC offset.

You cannot set the DC offset if you selected the Direct path. However, the output does still have some non zero offset. Refer to the <u>module</u> <u>specifications</u> for information about the maximum value of the DC offset.

# NI 5412 Output Impedance

The NI 5412 Analog Out path is designed to have an output impedance of 50  $\Omega$  from the Output Enable relay looking back towards the Main DAC. There is a selectable 25  $\Omega$  resistance that can be switched into the Analog Output path between the Output Enable Relay and the CH 0 SMB connector for applications requiring a 75  $\Omega$  impedance. Most applications use a load impedance of 50  $\Omega$ , but applications such as video testing, require 75  $\Omega$ . Refer to the following figure.



### Legend

If the load impedance is a high impedance (~1 M $\Omega$ ), you may see output levels up to twice the selected output value for a matched input/output impedance. These levels can be as high as 24 V_{pk-pk} for the High-Gain Amplifier path. Normally, the output levels increase as the load impedance increases. The NI 5412 can compensate for different load impedance values. Refer to <u>CH 0 Connector</u> for more information.

You can select an output impedance of 50  $\Omega$  or 75  $\Omega$ . Refer to the <u>niFgen</u> <u>Configure Output Impedance</u> VI or <u>niFgen_ConfigureOutputImpedance</u> function topics for more information.



**Note** The NI 5412 uses mechanical relays to switch between the 50  $\Omega/75 \Omega$  switch states. When you change a setting that results in a relay to switch, the bouncing of electromechanical relays on the NI 5412 interrupts the output signal for up to 10 ms.

# NI PXI-5412/5421/5422/5441/5442 Clock Source and Frequency

The NI 5412/5421/5441/5442 has a Sample clock rate of 10 Hz to 100 MHz and the NI 5422 has a Sample clock rate of 5 MHz to 200 MHz. The timing of the modules is very flexible, and you have multiple choices for deriving the Sample clock. There are modes for deriving the Sample clock from the internal Sample clock timebase, as well as modes to provide external clocks. You also have several choices for providing the frequency reference for the onboard phase-locked loop.



Note The male VHDCI (DIGITAL DATA & CONTROL) connector is not available on the NI 5412/5442 or on the NI 5421/5422 with the 8 MB memory option.

### **Related Topics**

Sample Clock Sources Internal Sample Clock Sources Phase-Locked Loop Reference Clock Sources External Sample Clock Sources Exporting Clocks

# NI 5412 Sample Clock

Waveform generation is driven by the Sample clock and, depending on your application, some sources may be better choices than others. You can use the following sources for the NI 5412 clock to derive the Sample clock:

- Internal Sample Clock—the Sample clock is derived from the Sample clock timebase via either divide by N or High-Resolution clock mode.
- External Sample Clock—the Sample clock is driven directly from an external source.
- Reference Clock—the Sample clock is derived from an external source that is phase-locked to the Sample clock timebase.

The following table shows the valid NI-FGEN property or attribute value combinations that can be used to configure the NI 5412/5421/5422/5441/5442 clock settings for an internal Sample clock, an external Sample clock, or a Reference clock. The term *Update clock* is synonymous with *Sample clock*.

Sample Clock Source [*]	Clock Mode*	PLL Reference Clock Source [*]
"OnboardClock"	NIFGEN_VAL_DIVIDE_DOWN	"None"
(default)		"PXI_CLK10" (PXI), "RTSI7" (PCI)
		"ClkIn" / "RefIn"
		"OnboardRefClk" (PCl)
	NIFGEN_VAL_HIGH_RESOLUTION	"None"
		"PXI_CLK10" (PXI), "RTSI7" (PCI)
		"ClkIn" / "RefIn"

		"OnboardRefClk" (PCI)
	NIFGEN_VAL_AUTOMATIC	"None"
	(default)	"PXI_CLK10" (PXI), "RTSI7" (PCI)
		"ClkIn" / "RefIn"
		"OnboardRefClk" (PCl)
"ClkIn"	Not Applicable	Not Applicable
"PXI_Star"		
"PXI_Trig<06>"		
*These column headings refer to NI-FGEN properties and attributes and the values in the columns represent the values that can be set on these properties or attributes. Settings that line up horizontally show valid combinations of the NI-FGEN attribute settings.		

### Sample Clock Source

The Sample Clock source is the clock from which the Sample clock is derived, and is used to drive the DAC and all waveform generation operations on the device. The default NI-FGEN setting for Sample clock source that drives the Sample clock is Internal. The Sample clock source only needs to be configured during applications that require an external Sample clock.

The NI 5412 supports five options for the Sample clock source: Internal and three External Sources for PXI and two External sources for PCI. The fundamental clock source for your waveform generation application is the Sample clock timebase. The NI 5412 provides a high-precision 100 MHz Voltage Controlled Crystal Oscillator (VCXO) internal source from which all waveform generation operations are derived. The External Sources are the NI 5412 CLK IN front panel connector, PXI_STAR (PXI), PXI_Trig<0..6> (PXI), and the RTSI<0..6> (PCI) lines.

For more information about configuring the Sample clock source for an External sample clock, refer to <u>External Sample Clock Sources</u>.

### **Clock Mode**

The clock mode determines the method of deriving the Sample clock from the Sample clock timebase. The clock mode is only applicable when using an internal Sample clock.

There are three options for setting the clock mode on your NI 5412: Divide-Down Sampling, High-Resolution Sampling, and the Automatic mode. The default NI-FGEN setting for clock mode is Automatic. The Automatic mode setting in NI-FGEN switches between the Divide-Down and the High-Resolution mode depending on the configured Sample clock rate.

For more information about configuring the clock mode, refer to <u>Internal</u> <u>Sample Clock Sources</u>.

### **PLL Reference Clock Source**

The PLL Reference clock source controls the source of the control voltage that tunes the VCXO of the Sample clock timebase for internal clock update sources. The phase-locked loop (PLL) circuit adjusts the Sample clock timebase VCXO to synchronize to a Reference clock.

The frequency stability of the Sample clock timebase matches that of the PLL Reference clock when the two are phase-locked. Phase-locking also synchronizes clocks of multiple devices that are phase locked to the same Reference clock.

There are three PXI options and four PCI options for selecting the PLL Reference Clock source on the NI 5412: Internal, PXI_CLK10 (PXI), RTSI7 (PCI), Onboard Reference Clock (PCI), and CLK IN. The default NI-FGEN setting for Reference Clock Source is Internal.

For more information about the NI 5412 phase-locked loop circuit, refer to <u>PLL Reference Clock Sources</u>.

# NI 5412/5421/5441/5442 Internal Sample Clock

The NI 5412/5421/5441/5442 can derive a Sample clock from its main internal timing source—the Sample Clock Timebase. The signal generator provides a high-precision 100 MHz Voltage Controlled Crystal Oscillator (VCXO) clock source for the Sample Clock Timebase. As shown in the following figure, the Sample Clock Timebase frequency is tuned by an Internal Calibration DAC control voltage when the <u>Reference Clock Source</u> property or the

NIFGEN ATTR REFERENCE CLOCK SOURCE attribute is set to "None". The Internal Calibration DAC, which is calibrated at the factory and which you also can calibrate, provides for the Sample Clock Timebase to maintain a high quality frequency source.



There are two methods, referred to as clock modes, for creating an internal Sample clock from the Sample Clock Timebase: Divide-Down (Divide by *N*) Sampling and High-Resolution Sampling.

In Divide-Down Sampling mode, the Divide by *N* circuit uses the Sample clock timebase of 100 MHz to create the frequency available for use as the Sample clock. Divide-Down Sampling mode can generate any internal timebase frequency of 100 MHz/*N*, where *N* is any integer from 1 to 4,194,304. For example, the internal timebase can run at 100 MHz, 50.0 MHz, 33.33 MHz, 25.0 MHz, 20.0 MHz, 16.666 MHz, and so on. The low frequency limit in Divide-Down Sampling mode is 23.84185 (100 MHz/4,194,304) Hz. Divide-Down Sampling mode provides a high-quality clock with the lowest jitter.

The High-Resolution Sampling mode also uses the Sample clock timebase at 100 MHz to generate a frequency from 10 Hz to 100 MHz. In addition, the High-Resolution mode uses direct digital synthesis to

generate very fine resolution increments on the order of microhertz. Refer to the <u>module specifications</u> for more information.

The following table, a subset of the table in <u>Sample Clock Sources</u>, shows the valid NI-FGEN property or attribute value combinations that can be used to configure the NI 5412/5421/5422/5441/5442 clock settings for an internal Sample clock. Refer to the <u>niFgen Configure</u> <u>Clock Mode</u> VI or the <u>niFgen_ConfigureClockMode</u> function for more information about setting up the clock.

Sample Clock Source	Clock Mode	PLL Reference Clock Source
"OnboardClk"	NIFGEN_VAL_DIVIDE_DOWN	"None" (default)
(default)	NIFGEN_VAL_HIGH_RESOLUTION	
	NIFGEN_VAL_AUTOMATIC (default)	

You can specifically set the clock mode for either Divide-Down Sampling or High-Resolution Sampling. Alternatively, you can select Automatic mode, which has NI-FGEN switch between the Divide-Down Sampling and High-Resolution Sampling mode, depending on the configured sample rate. NI-FGEN chooses the Divide-Down Sampling mode if the configured frequency exactly matches one of the possible divide-down frequencies. If the configured frequency does not match one of the possible divide-down frequencies, the High-Resolution Sampling mode is selected to provide the Sample clock frequency.

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**Note** The jitter of the High-Resolution clocking mode is frequency–dependent. At low frequencies the jitter increases. Refer to the <u>device specifications</u> for more information.

# NI 5412 External Sample Clock

The NI 5412 can accept an external clock to directly drive the Sample clock. In the case of an external Sample clock, the frequency stability and accuracy of the Sample clock is determined by the provided external Sample clock.



There are three external Sample clock sources for PXI and two external Sample clock sources for PCI to be the Sample clock for the NI 5412: CLK IN on the front panel, the PXI_STAR and PXI_Trig<0..7> lines on the PXI trigger bus, or the RTSI<0..7> (PCI) lines.

Refer to the <u>Configure Sample Clock Source</u> VI or the <u>niFgen_ConfigureSampleClockSource</u> function for more information about setting up the clock source.

The following table is a subset of the table in <u>Sample Clock Sources</u>, and shows the valid NI-FGEN property and attribute values and combinations to configure the NI 5412 clock settings for an external Sample clock.

Sample Clock Source	Clock Mode	PLL Reference Clock
ClkIn	Not Applicable	Not Applicable
PXI_Star		
PXI_Trig<07> RTSI<07> (PCI)		

You should configure the Sample clock rate when using an external

Sample clock. Refer to the <u>niFgen Set Sample Rate</u> VI or <u>niFgen_ConfigureSampleRate</u> function topics for more information about setting the Sample clock rate.



**Note** Refer to the <u>module specifications</u> for the allowable voltages, signal types, and clocks that you can use as an external Sample clock for all external Sample clocks.

## **External Sample Clock Considerations**

The NI 5412 incorporates high-speed digital clocking technology, and requires a stable, free-running Sample clock to operate properly. When the NI 5412 is committed—either explicitly by calling <u>niFgen Commit</u> VI or the <u>niFgen Commit</u> function or implicitly by writing waveforms or sequences or Initiating a generation—the external Sample clock must be available to the device. If the external clock becomes unstable due to glitching, changing frequency, or is removed entirely, NI-FGEN returns a hardware clocking error.

Refer to the <u>NI-FGEN Programming State Model</u> for more information.

If necessary, you can change the rate or the source of the external Sample clock between subsequent generations by first calling the <u>niFgen</u> Abort Generation VI or the <u>niFgen_AbortGeneration</u> function, changing the rate or source, and then calling niFgen_Commit. NI-FGEN re-programs the NI 5412 for the new settings, and you can call the <u>niFgen_Initiate</u> Generation VI or <u>niFgen_InitiateGeneration</u> function to start the next generation.

If you must remove the external Sample clock between generations (after niFgen Abort, but before niFgen Initiate), but are not changing the frequency or source of the external clock, you have two options:

- 1. Call niFgen Initiate, which returns a hardware clocking error because the external Sample clock is gone, then clear the error and call niFgen Initiate again—causing NI-FGEN to reprogram the hardware to use the external clock again.
- 2. Force the device to be re-committed by changing some attribute to another value and then back to its original value. This action causes NI-FGEN to re-commit the settings to hardware, which would not have happened otherwise because NI-FGEN would not have known that the external Sample clock was gone.

**Caution** When configuring an external Sample clock, you must set the sample rate to the exact frequency your are using to avoid data errors. Refer to the <u>niFgen Set Sample Rate</u> VI or <u>niFgen_ConfigureSampleRate</u> function topics for more information.

# NI 5412/5421/5422/5441/5442 Phase-Locked Loop Reference Clock

A phase-locked loop (PLL) is a circuit that tunes the Sample clock timebase to phase–lock to an external Reference clock. The frequency stability and accuracy of the Sample clock timebase matches that of the Reference clock when they are phase–locked. Using the PLL on your device enables you to frequency-lock multiple devices in a single chassis or devices in separate chassis.

Note Refer to the <u>device specifications</u> for information about the phase-locked loop reference frequencies available on your device.

The following figure shows the NI 5412/5421/5422/5441/5442 Reference Clock Source path.



### Legend

To begin the PLL, the phase comparator compares the selected Reference clock to the 100 MHz (or 200 MHz for the NI 5422) clock of the Sample clock timebase. Next, a control voltage proportional to the phase difference between the two clocks is developed and used to tune the Sample clock timebase into alignment with the Reference clock. Finally, the Sample clock timebase output is routed back to the phase comparator, closing the loop.

 $\overline{\mathbb{Z}}$ 

**Note** When the <u>Reference Clock Source</u> property or the <u>NIFGEN_ATTR_REFERENCE_CLOCK_SOURCE</u> attribute is set to

"None"; the internal calibration DAC generates the calibration voltage, and the PLL circuit is not used.

## **Reference Clock Sources**

The NI 5412/5421/5422/5441/5442 can phase–lock its Sample clock timebase to an external signal that is present on the CLK IN front panel connector. PXI devices can also phase–lock to a 10 MHz Reference clock signal provided by the PXI bus (PXI_CLK10), while PCI devices can phase–lock to RTSI line 7 or to the onboard Reference clock.

The following table is a subset of the table in <u>Sample Clock Sources</u>, and shows the valid NI-FGEN property value combinations that can be used to configure the NI 5412/5421/5422/5441/5442 clock settings for an external Reference clock. The attributes that correspond to these properties are NIFGEN_ATTR_SAMPLE_CLOCK_SOURCE,

NIFGEN_ATTR_CLOCK_MODE, and

NIFGEN_ATTR_REFERENCE_CLOCK_SOURCE. The valid attribute value combinations will reflect the valid property combinations.

Sample Clock Source	Clock Mode	PLL Reference Clock Source
"OnboardClock" (default)	NIFGEN_VAL_DIVIDE_DOWN	"None"
		"PXI_CLK10", "RTSI7"
		"ClkIn", "RefIn"
		"OnboardRefClk"
	NIFGEN_VAL_HIGH_RESOLUTION	"None"
		"PXI_CLK10", "RTSI7"
		"ClkIn", "RefIn"
		"OnboardRefClk"
	NIFGEN_VAL_AUTOMATIC	"None"
	(default)	"PXI_CLK10", "RTSI7"
		"ClkIn", "RefIn"
		"OnboardRefClk"

Note Refer to the <u>device specifications</u> for information about available signal levels on the CLK IN front panel connector.

Refer to the <u>niFgen Configure Reference Clock</u> VI or the <u>niFgen_ConfigureReferenceClock</u> function for more information about configuring the Reference clock.

# NI 5412 Exporting Clocks

The NI 5412 provides two resources for exporting your clocks and multiple destinations to route to.



The following table shows the available clock signals that can be routed to devices external to the NI 5412, the labels NI-FGEN uses to describe them and the destination options.

Clock to be Exported	Destination Options
Sample Clock	PFI<01> SMB connector
	PXI_Trig<06> (PXI), RTSI<06> (PCI)
Sample clock timebase	PFI<01> SMB connector
	PXI_Trig<06> (PXI), RTSI<06> (PCI)
Reference Clock	PFI<01> SMB connector
	PXI_Trig<06> (PXI), RTSI<06> (PCI)
Onboard Reference Clock	RTSI7

## Sample Clock

For synchronization purposes, the NI 5412 allows you to export your Sample clock so that other devices can have the same timing as the NI 5412. The Sample clock can be routed to the PFI<0..1> front panel SMB connectors, PXI_Trig<0..6> lines on the PXI trigger bus, or the RTSI<0..6> (PCI) lines.

Additionally, the exported clock can be divided down by an integer value (no less than 2) before being exported to the PFI<0..1> SMB connectors, PXI_Trig<0..6> lines, or the RTSI<0..6> (PCI) lines. Refer to the Exported Sample Clock Divisor property or the

<u>NIFGEN_ATTR_EXPORTED_SAMPLE_CLOCK_DIVISOR</u> attribute for more information about configuring the Sample clock divisor.

### Sample Clock Timebase

For synchronization purposes, the NI 5412 allows you to export your Sample clock timebase so that other devices can have the same timing as the NI 5412. The Sample clock timebase can be routed to the PFI<0..1> SMB connectors on the front panel, the PXI_Trig<0..6> lines on the PXI trigger bus, or the RTSI<0..6> (PCI) lines.

Additionally, the exported clock can be divided down by an integer value before being exported to the PFI<0..1> SMB connectors, the PXI_Trig<0..6> lines, or the RTSI<0..6> (PCI) lines. Refer to Exported Sample Clock Timebase Divisor property or the NIFGEN_ATTR_EXPORTED_SAMPLE_CLOCK_TIMEBASE_DIVISOR attribute for more information about configuring the Sample clock divisor.

## **Reference Clock**

For synchronization purposes, the NI 5412 allows you to export your PLL Reference clock so that other devices can lock their clock sources to the same signal. Referring to the previous image, this clock is the actual clock that is configured for the NI 5412 phase-locked loop circuit to use as a reference. You must have a Reference clock configured as a PLL Reference Clock source for the signal to be available for exporting. The Reference clock can be routed to the PFI<0..1> SMB connectors on the front panel, the PXI_Trig<0..6> lines on the PXI trigger bus, or the RTSI<0..6> (PCI) lines.



**Note** Although NI-FGEN allows values for Reference clock frequency on the NI 5412 from 1 MHz to 20 MHz in 1 MHz increments, the NI 5412 specifications are only valid with Reference clock frequencies from 5 MHz to 20 MHz.

## **Onboard Reference Clock**

The onboard Reference clock is a dedicated 10 MHz clock for PCI modules only. The onboard Reference clock can only be exported to RTSI7, for other modules to use, and to reimport as the Reference clock. You can export the onboard Reference clock to other modules on RTSI7 and then reimport it so that all devices (including the master) can use the same Reference clock.
### **Destination Options**

**PFI<0..1>**—The Sample clock and the Reference clock can be exported to the PFI 0 and PFI 1 SMB connectors on the front panel to synchronize external devices. You must configure the device to export the desired clock to the PFI SMB connectors.



**Note** PFI 0 is optimized to have lower jitter than PFI 1 for exporting the Sample clock or the Reference clock.

**PXI_Trig<0..6>**—The Sample clock and the Reference clock can be exported to the PXI_Trig lines or RTSI (PCI) lines. The PXI/PCI standard allows for devices to route signals to other devices in your PXI chassis to enhance device to device synchronization. Refer to the chassis documentation for specifications to ensure the reference signal is within tolerance. You must configure the device to export the desired clock to the PXI_Trig line or RTSI line. When exporting signals, PXI_Trig<0..6> are equivalent to RTSI_<0..6>.

Refer to the <u>niFgen Export Signal</u> VI or the <u>niFgen_ExportSignal</u> function for more information about configuring the destinations for the desired clock signal.

## NI 5412/5421/5422/5441/5442 Onboard Memory

NI 5412/5421/5422/5441/5442 signal generators use an onboard memory that is 16-bits wide. The minimum standard memory size for the NI 5412/5421/5422/5441/5442 is 8 Mbytes which translates to 8,338,608 usable bytes. With the minimum standard memory size, you can store very long waveforms on the device and obtain reliable waveform generation at full sample rate of 100 MS/s (or 200 MS/s for the NI 5422). The NI 5421/5422/5441/5442 also comes with higher memory options of 32 Mbytes, 256 Mbytes, and 512 Mbytes. The NI 5412 comes with higher memory options of 32 Mbytes and 256 Mbytes.

The onboard memory is a single large memory area that stores both waveforms and sequence instructions to generate the waveforms. The instructions for a complicated sequence can occupy a significant portion of memory. The architecture of the NI 5412/5421/5422/5441/5442 allows you to load multiple waveforms and multiple sequence instructions into the memory. The following diagram illustrates

NI 5412/5421/5422/5441/5442 memory allocation. A number of waveforms are stored in the onboard memory ranging from 1 to n; there are also a number of sequence instructions ranging in number from 1 to m. The values of n and m depend on the waveform and instructions configured and are ultimately limited by the amount of memory.

Wave form 1	Waveform 2	•••	Waveform n	Sequence Instructions 1	Sequence Instructions 2	• • •	Sequence Instructions m	Free Memory
----------------	---------------	-----	---------------	-------------------------------	-------------------------------	-------	-------------------------------	----------------

The following tables list the types of information that are used to make up the instructions that are saved to memory. You can store the instructions for multiple sequences to the onboard memory ahead of time and generate them later, allowing for quick reconfiguration times between tests. There are two example sequences. The first table, Sequence 1, represents the instructions for a sequence containing a maximum number of segments *k*. The second table, Sequence m, is an example of a sequence containing 8 segments. Each sequence uses different waveforms that are downloaded to the onboard memory, as well as various looping and Marker placement options to construct each resulting

waveform.

Sequer	Sequence 1: Burst Trigger Mode					ice <i>m</i> : Step	oped Tr
Sequence Segment	Waveform	# of Loops	Marker Placement		Sequence Segment	Waveform	# of Loop:
1	1	1	0		1	1	1
2	5	14	100		2	2	340
3	17	1	-1		3	35	1
4	12	18,045	10,000		4	2	10
5	12	64,000	12		5	340	5
6	34	64,000	0		6	34	64,00
					7	20,000	1,000,0
k	15	20	10,000		8	1	1

## NI 5412/5421/5422/5441/5442 Waveform and Generation Instruction Memory Size

### Waveform Memory Size

Waveforms are stored in the NI 5412/5421/5422/5441/5442 onboard memory in contiguous blocks. These blocks are allocated in multiples of 128 bytes. This allocation style means that while waveform sizes may be multiples of four samples (eight bytes) on the NI 5412/5421/5422/5441 and one sample (two bytes on the NI 5442), the amount of onboard memory allocated for each waveform is a multiple of 128 bytes. The following figure represents the total memory of a device and shows memory that was initially empty, but it now has multiple waveforms written to it, nearly filling the device memory.

Waveform Wave 1 2	form •••	Waveform n	Sequence Instructions 1	Sequence Instructions 2	• • •	Sequence Instructions m	Free Memory
----------------------	----------	---------------	-------------------------------	-------------------------------	-------	-------------------------------	----------------

The amount of memory that a waveform takes up in the onboard memory is relatively easy to calculate using the following two rules.

- 1. Each sample in the waveform uses two bytes of memory space. Four bytes are used when the onboard signal processing block is enabled and the <u>Data Processing Mode</u> property is set to Complex or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> is set to NIFGEN_VAL_OSP_COMPLEX.
- 2. Memory is written to in blocks of 128 bytes (2 bytes on the 5442).

Calculate the memory size by multiplying the number of samples in the waveform by two (or four) and then rounding this value up to the nearest multiple of 128.

#### Examples

- 1. A waveform containing 16 samples occupies 32 bytes in memory. By rounding up to the nearest multiple of 128, you can determine that the waveform occupies 128 bytes in memory.
- 2. A waveform containing 64 samples occupies 128 bytes in memory. By rounding up to the nearest multiple of 128, you can determine that the waveform occupies 128 bytes in memory.
- 3. A waveform containing 68 samples occupies 136 bytes in

memory. By rounding up to the nearest multiple of 128, you can determine that the waveform occupies 256 bytes in memory.

- 4. A waveform containing 10,000 samples occupies 20000 bytes in memory. By rounding up to the nearest multiple of 128, you can determine that the waveform occupies 20,096 bytes in memory.
- 5. A waveform containing 64 complex samples occupies 256 bytes in memory. By rounding up to the nearest multiple of 256, you can determine that the waveform occupies 256 bytes in memory. This example is only possible with the onboard signal processing block enabled.

#### **Instruction Memory Size**

The NI 5412/5421/5422/5441/5442 uses a waveform generation engine that processes instructions that govern how a waveform or a sequence of waveforms is generated. These instructions determine which waveforms are generated, how the device responds to triggers, how many times a waveform is looped, when Marker events are generated, and so forth. The instructions depend on the output mode, trigger mode, trigger source, waveforms in onboard memory, and sequence lists that are configured. The instructions are stored in the onboard memory along with the waveform data. The calculations to determine the instruction size that is stored in the onboard memory depends on the NI-FGEN output mode and the NI-FGEN trigger mode. The following table includes basic equations for determining the amount of memory, in bytes, that are used for the different generation configurations.

Instruction Memory Size* Formulae				
Arbitrary Waveform Mode	Size in bytes = 256 per waveform			
Arbitrary Sequence Mode	Stepped: Size in bytes = 208 + (80 * <i>N</i> )			
<i>N</i> = Number of segments in sequence	Continuous: Size in bytes = 208 + (64 * <i>N</i> )			
	Single: Size in bytes = $80 + (64 * N)$			
	Burst: Size in bytes = 160 + (128 * <i>N</i> )			
*The instruction size in memory is the size, in bytes, rounded up to the nearest multiple of 128 bytes.				

#### Examples

- 1. The memory size required to generate a waveform in Arbitrary Waveform mode is always 256 bytes of onboard memory for that specific waveform. Each waveform that is saved to onboard memory uses 256 byes of memory for instructions.
- 2. The memory size required to generate a waveform using Arbitrary Sequence mode and Stepped trigger mode with 50 segments in a sequence list is determined by the following formula:

Size in Bytes =  $208 + (80 \times 50) = 4,208$  bytes.

Size in memory = 4208 coerced up to the next multiple of 128 = 4,224 bytes.

3. The memory size required to generate a waveform using Arbitrary Sequence mode and Continuous trigger mode with 500 segments in a sequence list is determined by the following formula:

Size in Bytes =  $208 + (64 \times 500) = 32,208$  bytes.

Size in memory = 32,208 coerced up to the next multiple of 128 = 32,256 bytes.

4. The memory size required to generate a waveform using Arbitrary Sequence mode and Single trigger mode with 1,003 segments in a sequence list is determined by the following formula:

Size in Bytes =  $80 + (64 \times 1,003) = 64,272$  bytes.

Size in memory = 64,272 coerced up to the next multiple of 128 = 64,284 bytes.

5. The memory size required to generate a waveform using Arbitrary Sequence mode and Burst trigger mode with 2345 segments in a sequence list is determined by the following formula:

Size in Bytes =  $160 + (128 \times 2,345) = 300,320$  bytes.

Size in memory = 300,320 coerced up to the next multiple of 128 = 300,416 bytes.

#### **Total Memory Size**

The following examples show how to calculate total memory for an application. The examples use each of the four trigger modes for the Arbitrary Sequence mode and use varying numbers of waveforms, waveform sizes, and number of segments in the sequences.

Note The following examples only consider the memory used for instructions for one sequence. It is possible to create and save to memory the instructions for as many sequences as the available free memory allows.

#### Examples

1. An application requires using three waveforms with the following sizes: 72, 132, and 260 samples. The waveforms are generated by using Arbitrary Sequence mode and Single trigger mode to configure 20,000 segments in a sequence list. The following tables show all the numbers used to determine the total memory stored in the onboard memory: 1,281,408 bytes.

Waveforms	Samples	Bytes	Rounded Size
А	72	144	256
В	132	264	384
С	260	520	640
	1,280		

Number of Segments in	Memory	Bytes	Rounded
Sequence	Calculation		Size
20,000	80 + (64 * 20,000) =	1,280,080	1,280,128

**Total Onboard Memory Used** = 1,281,408 bytes

2. An application requires using six waveforms with the following sizes: 480, 260, 960, 492, 516, and 604 samples. The waveforms are generated by using Arbitrary Sequence mode and Burst trigger mode to configure 10,000 segments in a sequence list. The following table shows all the numbers used to determine the total memory stored in the onboard memory: 135,296 bytes.

Waveforms	Samples	Bytes	Rounded Size
А	480	960	1,024
В	260	520	640
С	960	1,920	1,920
D	492	984	1,024
E	516	1,032	1,152
F	604	1,208	1,280
	7,040		

Number of Segments in	Memory	Bytes	Rounded
Sequence	Calculation		Size
10,000	160 + (128 * 10,000) =	128,160	128,256

#### Total Onboard Memory Used = 135,296 bytes

An application requires using five waveforms with the following sizes: 10,000; 1,000,000; 2,000,000; 30,000,000; and 5,000 samples. The waveforms are generated by using Arbitrary Sequence mode and Stepped trigger mode to configure 2,000 segments in a sequence list. The following table shows all

the numbers used to determine the total memory stored in the onboard memory: 66,190,464 bytes.

Waveforms	Samples	Bytes	<b>Rounded Size</b>
A	10,000	20,000	20,096
В	1,000,000	2,000,000	2,000,000
С	2,000,000	4,000,000	4,000,000
D	30,000,000	60,000,000	60,000,000
E	5,000	10,000	10,112
	66,030,208		

Number of Segments in	Memory	Bytes	Rounded
Sequence	Calculation		Size
2,000	208 + (80 * 2,000) =	160,208	160,256

**Total Onboard Memory Used** = 66,190,464 bytes

4. An application requires using seven waveforms with the following sizes: 1,000; 2,000; 2,000, 10,000; 20,000; 500; and 260 samples. The waveforms are generated by using Arbitrary Sequence mode and Continuous trigger mode to configure 100 segments in a sequence list. The following table shows all the numbers used to determine the total memory stored in the onboard memory: 78,720 bytes.

Waveforms	Samples	Bytes	Rounded Size
А	1,000	2,000	2,048
В	2,000	4,000	4,096
С	2,000	4,000	4,096

D	10,000	20,000	20,096
E	20,000	40,000	40,064
F	500	1,000	1,024
G	260	520	640
	72,064		

Number of Segments in	Memory	Bytes	Rounded
Sequence	Calculation		Size
100	208 + (64 * 100) =	6,608	6,656

#### **Total Onboard Memory Used** = 78,720 bytes

5. An application requires using seven complex waveforms with the following sizes: 500; 1,000; 1,000, 5,000; 10,000; 250; and 130 samples with the <u>OSP block</u> enabled and the Data Processing Mode property set to Complex or the NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE attribute set to NIFGEN_VAL_OSP_COMPLEX. Additionally, the signal generator is configured for Arbitrary Sequence mode and Continuous trigger mode with 100 segments in a sequence list. The following table shows all the numbers used to determine the total memory stored in the onboard memory: 78,720 bytes.

Waveforms	Samples	Bytes	<b>Rounded Size</b>
A	500	2,000	2,048
В	1,000	4,000	4,096
С	1,000	4,000	4,096
D	5,000	20,000	20,096
E	10,000	40,000	40,064

Memory Size =		72,064	
G	130	520	640
F	250	1,000	1,024

Number of Segments in	Memory	Bytes	Rounded
Sequence	Calculation		Size
100	208 + (64 * 100) =	6,608	6,656

Total Onboard Memory Used = 78,720 bytes

## NI 5412/5421/5422/5441/5442 Memory Fragmentation

When storing multiple waveforms in NI 5412/5421/5422/5441/5442 memory, fragmentation can become a problem. Both waveforms and instructions are stored in NI 5412/5421/5422/5441/5442 memory in contiguous blocks. These blocks are allocated in multiples of 128 bytes, and they are written in the order that you configure them. Fragmentation occurs when you delete a waveform or script from memory that was not the last block written.

Every new NI-FGEN session begins with empty memory. First, multiple waveforms are written to memory, nearly filling the device memory, as shown in the following diagram.



If you now try to write Waveform 5 (pictured in the following figure) to the device, you find there is not enough memory. To make room for the waveform, you could delete waveform 3 to create enough space in memory for Waveform 5.



Unfortunately, though you now have enough free memory space for Waveform 5, this space is fragmented, so you must also clear and redownload all waveforms and generation instructions following the deleted waveform. The following figure illustrates the result.

Waveform 1	VVave form 2	VVave form 4	Wave form 5	Sequence Instructions	F r e
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### NI 5412/5421/5422/5441/5442 Arbitrary Waveform Generation Mode

Arbitrary Waveform generation mode generates waveforms from usercreated/provided waveform arrays of numeric data. The waveform arrays are downloaded to the arbitrary waveform generator onboard memory. Arbitrary Waveform generation mode also uses memory to store the instructions for generating waveform sequences in the onboard memory. The timing and behavior of arbitrary waveform generation is dependent on the <u>trigger mode</u> you select.

## NI 5412/5421/5422/5441 Sample Size and Resolution

The NI 5412/5421/5422/5441 stores arbitrary waveforms in memory as signed 16-bit digital words. On the NI 5421/5422/5441, the entire 16 bits are sent to the digital gain circuit, the digital filter and the DAC. On the NI 5412, the upper 14 bits are sent to the digital gain circuit, the digital filter, and the DAC.

The NI 5441 stores arbitrary *complex* waveforms in memory as interleaved real/imaginary 16-bit digital words. Each real/imaginary pair is processed by the OSP block before it is sent to the digital gain circuit, the digital filter, and the DAC.

#### **Related Topics**

**Onboard Memory** 

Waveform Sizes

# NI 5412/5421/5422/5441 Minimum Waveform Size and Quantum

#### Waveform Size

The NI 5412/5421/5422/5441 onboard memory architecture imposes certain requirements on the waveform size and quantum. The minimum waveform size depends on the output mode and the <u>Trigger Mode</u>. Refer to the <u>module specifications</u> for the minimum waveform size values for the different modes.

Note To provide greater programming flexibility, NI-FGEN does not strictly enforce the minimum waveform sizes stated in the specifications. NI-FGEN enforces a minimum waveform size of four samples for all trigger modes (two if the onboard signal processing block is enabled and the <u>Data Processing Mode</u> property is set to complex or the

NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE attribute is set to NIFGEN_VAL_OSP_COMPLEX), so it is possible to generate waveforms that are smaller than the sizes given in the specifications. However, the device may not be able to fetch data from onboard memory fast enough to keep up with waveform generation at very high sample rates.

This condition may occur if a segment is looping over a very small waveform, if a segment is generating a marker within a very small waveform, or if triggers are advancing the segments in a sequence very rapidly. When this occurs, NI-FGEN reports **Error** – **1074115901 (0xBFFA4AC3): Device Data Underflow**.

The simplest way to avoid this condition is to follow the minimum waveform size guidelines in the specifications. If these rules are followed, a data underflow error will not occur under any sample rate. You may be able to develop applications that generate waveforms smaller than those listed in the specifications at slower sample rates. If a data underflow occurs, NI-FGEN reports the error when the generation is aborted, which is typically done by calling the niFgen Abort Generation VI or the niFgen_AbortGeneration function, or if you call the niFgen Wait Until Done, or niFgen Is Done VIs (or the niFgen_WaitUntilDone or niFgen_IsDone functions) while the device is generating a signal. To

monitor error conditions during waveform generation, the niFgen Is Done VI or the niFgen_IsDone function can be called repeatedly while the device is generating a signal.

### Quantum

Quantum is the increment in samples that waveform sizes must adhere to. Waveforms must be downloaded in integer multiples of the four samples (or two for complex samples), the quantum for the NI 5412/5421/5422/5441.

For example, if in Arbitrary Waveform mode, you request to load a waveform of seven samples, the task will not complete successfully because the waveform is not an integer multiple of the quantum size. Waveform sizes that meet the conditions include 4, 8, 12, 16, 20, and so on, up to maximum allowable waveform size.

The maximum waveform size allowed depends on the remaining available space in the onboard memory of the device. The remaining available space depends on factors such as any waveforms and generation instructions currently occupying memory space in the onboard memory. The maximum allowable size equals the memory size of the device minus the data already in memory. Query Max Waveform Size property or the <u>NIFGEN_ATTR_MAX_WAVEFORM_SIZE</u> attribute for the current largest size waveform that can be downloaded to the device.

You can download floating point, signed 16-bit binary, or complex floating-point waveforms to the devices Onboard Memory. LabVIEW programmers can refer to <u>niFgen Create Waveform</u> or <u>niFgen Write</u> <u>Waveform</u> VIs for more information. C programmers can refer to <u>niFgen_CreateWaveformF64</u>, <u>niFgen_CreateWaveformI16</u>, <u>niFgen_CreateWaveformComplexF64</u>, <u>niFgen_WriteWaveform,</u> <u>niFgen_WriteBinary16Waveform</u>, or <u>niFgen_WriteWaveformComplexF64</u> functions for more information.

## NI 5412/5421/5422/5441/5442 Arbitrary Waveform Generation Trigger Modes

This topic contains information about the behavior of the signal generator in Arbitrary Waveform Generation mode with a particular trigger mode.

### **Single Trigger Mode**

The waveform you downloaded generates only once and waveform generation halts, unless the <u>Arbitrary Waveform Repeat Count</u> property or the <u>NIFGEN_ATTR_ARB_REPEAT_COUNT</u> attribute is set, in which case the waveform generates the specified number of times. Once the last waveform generates, the analog output indefinitely settles at the DC value of the last sample in the waveform. Only one Start trigger is required to start waveform generation. All Start triggers after the first Start trigger are ignored.



#### **Continuous Trigger Mode**

The waveform you downloaded generates continuously after receiving one Start trigger. All Start triggers after the first Start trigger are ignored.

Start Trigger Vaveform Repeats Continuously End of Waveform

### **Stepped Trigger Mode**

The waveform you downloaded generates each time a Start trigger occurs. After a waveform finishes generating, the last sample of the waveform repeats continuously until the next Start trigger is received. When the next Start trigger is received, the waveform generates again. If a Start trigger is received while a waveform is generating, the Start trigger is ignored and another Start trigger is required to regenerate the waveform after the last sample generates.



If the <u>Arbitrary Waveform Repeat Count</u> property or the <u>NIFGEN_ATTR_ARB_REPEAT_COUNT</u> attribute is set, the waveform generates the specified number of times instead of just once.

### **Burst Trigger Mode**

Burst trigger mode operates the same as Continuous trigger mode when the device is operating in Arbitrary Waveform mode.

# NI 5412/5421/5422/5441/5442 Generating Marker Events in Arbitrary Waveform Mode

To create a marker in <u>Arbitrary Waveform Mode</u>, set the <u>Arbitrary</u> <u>Waveform Marker Position</u> property or the <u>NIFGEN_ATTR_ARB_MARKER_POSITION</u> attribute. Then use the <u>niFgen Export Signal</u> VI or the <u>niFgen_ExportSignal</u> function to export the marker signal.

### NI 5412/5421/5422/5441/5442 Arbitrary Sequence Mode

You can load multiple waveforms in the onboard memory of the NI PXI-5412/5421/5422/5441/5442. A finite number of samples make a waveform. To generate these downloaded waveforms in a specific order, you must prepare a sequence, which contains a number of segments in a specific order. Each segment specifies a downloaded waveform, a number of loops to repeat the selected waveform, and a numeric offset in which a marker is generated by the device. The timing and behavior of the generation of a waveform sequence is dependent on the trigger mode selected.

The following figures show the concepts of waveforms and segment sequencing.

Waveform A

Waveform A represents a single cycle of a sine wave that is downloaded to onboard memory.

Waveform B

Waveform B represents a single cycle of a ramp waveform that is downloaded to onboard memory.



Waveform Segment 1 shows a segment created using Waveform A, repeating, or looping, three times.

Waveform Segment 2 (Loops = 2)

Waveform Segment 2 contains Waveform B looping two times.



Waveform Segment 3 contains Waveform A looping only once.



Sequence List (Waveform Linking)

These waveforms are linked in a sequence. The concept of using a sequence to generate waveforms is referred to as "waveform sequencing" or "linking and looping" waveforms.

### **Segment Components**

You create a sequence segment by segment. Each segment is made up of the four components shown in the following table.

Waveform Handle	Specifies the downloaded waveform to be accessed by the segment. A waveform handle is returned for each waveform that is downloaded to the onboard memory. Refer to the niFgen Create Waveform or niFgen Allocate Waveform VIs, or the niFgen_CreateArbWaveform or niFgen_AllocateWaveform functions for more information about downloading waveforms.
Sample Count	Specifies how many samples of a downloaded waveform the segment uses. The sample count may not be the actual size of the downloaded waveform. If the sample count is less than the actual size of the downloaded waveform, only a part of that waveform is used for that segment, starting with the first sample of the waveform. If the count is more than the actual size of that waveform, NI-FGEN sends an error. If the sample count is set to zero, NI-FGEN automatically uses the true size of that waveform.
Waveform loops	Specifies the number of times that the waveform (or portion indicated by sample count of the waveform) loops. The maximum number of loops is 16,777,215.
Marker offset	Specifies where the marker generates within that waveform. The offset is referenced to the beginning of the waveform, with sample 0 being the first sample of the waveform. For more information about markers, refer to <u>Markers</u> .

Refer to the <u>niFgen Create Arbitrary Sequence</u> or <u>niFgen Create</u> <u>Advanced Arb Sequence</u> VIs or the <u>niFgen_CreateArbSequence</u> or <u>niFgen_CreateAdvancedArbSequence</u> functions for more information about creating and configuring arbitrary sequences.

## NI 5412/5421/5422/5441/5442 Arbitrary Sequence Trigger Modes

This topic contains information about the behavior of the signal generator in Arbitrary Sequence mode with a particular trigger mode.

### **Single Trigger Mode**

The waveform pattern you define in the sequence list generates only once by going through the entire list and then the waveform generation halts. Only one Start trigger is required to start waveform generation. After the NI 5412/5421/5422/5441/5442 receives a Start trigger, the waveform generation starts at the first segment and continues through the last segment. After the entire sequence list has been generated, it remains at the DC level of the last sample of the last segment of the sequence indefinitely. All Start triggers after the first Start trigger that starts waveform generation are ignored.

Start Trigger Last Sample of Last Segment Generated Continuously End of All Segments

Note You can have the waveform finish generating at a desired DC value by making the last point in the last segment that DC value, or you can add an extra segment filled with the same DC value.

#### **Continuous Trigger Mode**

The waveform pattern you define in the sequence list generates continuously by continually cycling through the sequence list. Only one Start trigger is required to start waveform generation. After the device receives a Start trigger, the waveform generation starts at the first segment and continues through the last segment, and then loops back to the start of the first segment, continuing indefinitely. All Start triggers after the first Start trigger that starts waveform generation are ignored.

Start Trigger Sequence of Waveforms Repeated Continuously End of All Segments in Sequence List

### **Stepped Trigger Mode**

The waveforms you define in the sequence list generate one segment at a time, each time a Start trigger occurs. The waveform loops as many times as has been configured for that particular segment. After the generation of a segment has halted, the last sample of the waveform repeats continuously until the next Start trigger is received. When the next Start trigger is received, the waveform defined by the next segment generates for configured amount of loops. After the sequence list is exhausted, the waveform generation returns to the first segment and subsequent Start triggers restart the process. If a Start trigger is received while a waveform is generating, the Start trigger is ignored and another Start trigger is required to generate the next segment after the last sample generates. A Start trigger is recognized only after the segment finishes generating.



#### **Burst Trigger Mode**

Each waveform you define in the sequence list generates continuously until another Start trigger occurs. A Start trigger causes the waveform generation to switch to the waveform defined by the next segment, after the current waveform finishes. After the sequence list is exhausted, the waveform generation returns to the waveform defined by the first segment and subsequent Start triggers will restart the process. Only the first Start trigger which signals a transition to the next segment is recognized, all subsequent Start triggers are ignored until the currently generating waveform finishes.



Note The transition of one waveform to the next can be made amplitude continuous if waveforms in all segments start and end at the same amplitude. Alternatively, this also can be accomplished by ensuring that the waveforms from one segment to the next end and start at the same amplitude. This amplitude continuous transition is shown in the previous Arbitrary Sequence Mode examples by the transitions of Segments 1 to Segment 2, and Segment 3 to Segment 4. The transition from Segment 2 to Segment 3 shows a discontinuous transition, going from a positive value on the last sample of the ramp waveform right to a midrange value of the sine waveform.

# NI 5412/5421/5422/5441/5442 Generating Marker Events in Arbitrary Sequence Mode

To create a marker in <u>Arbitrary Sequence Mode</u>, refer to the **Marker** Location Array parameter of the <u>niFgen Create Advanced Arb</u> <u>Sequence</u> VI or the **markerLocationArray** parameter <u>niFgen_CreateAdvancedArbSequence</u> function. Then use the <u>niFgen Export</u> <u>Signal</u> VI or the <u>niFgen_ExportSignal</u> function to export the marker signal.
# NI 5412/5421/5422/5441/5442 Trigger Sources

Trigger sources are software selectable. You can use any of the following external input triggers:

- PFI 0 or PFI 1 on the SMB front panel connectors
- PFI 2 or PFI 3 on the DIGITAL DATA & CONTROL front panel connector (except NI 5412 and 5442)
- RTSI<0..7> (PCI) lines or PXI_TRIG<0..7> lines and PXI_STAR (except NI 5442) on the PXI trigger bus on the backplane

The following figure shows the possible trigger sources for the NI 5412/5421/5422/5441/5442.



Legend

[§]Refer to Exporting Signals for more information routing signals.

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**Notes** The male VHDCI (Digital Data & Control) connector is not available on the NI 5412, the NI 5421/5422 with the 8 MB memory option, or the NI 5442.

The PXI_STAR trigger line is not a valid trigger source on the NI 5442.

External triggers are only recognized on the rising edge of the trigger. All

triggers are ignored until you call the <u>niFgen Initiate Generation</u> VI or the <u>niFgen_InitiateGeneration</u> function.

The default trigger source for NI-FGEN is Immediate, which causes an automatic Start trigger pulse to be generated internally as soon as hardware can generate signals after generation has been initiated. You can configure the trigger source with <u>niFgen Configure Trigger</u> VI or the <u>niFgen_ConfigureTriggerSource</u> function. Refer to the <u>niFgen Send</u> <u>Software Edge Trigger</u> VI or the <u>niFgen_SendSoftwareEdgeTrigger</u> function for more information about programmatically triggering the device.

Refer to the <u>device specifications</u> for the minimum Start trigger pulse width required for operation.

#### **Related Topics**

PXI Trigger Lines

PXI Star Trigger Line

# NI PCI-5412/5421 Front Panel

The following figure shows the NI PCI-5412/5421 front panel. This front panel has four SMB connectors and an optional 68-pin male VHDCI connector. The male VHDCI (Digital Data & Control) connector is not available on the NI 5412 or the NI 5421 with the 8 MB memory option.



The <u>CLK IN Connector</u> SMB connector provides the device with an external reference or external Sample clock.

The <u>PFI 0 and PFI 1</u> SMB connectors are multi-direction connections for a number of different signals.

DIGITAL DATA & CONTROL is an optional 68-pin male VHDCI connector

that contains the 16-bit LVDS digital pattern outputs.

The  $\underline{CH 0}$  SMB connector is the analog output from which arbitrary waveforms are generated.

# NI PCI-5412 Theory of Operation

Expand this topic for information about the NI PCI-5412 theory of operation.

# NI PCI-5412 Block Diagram

This topic contains information about the NI PCI-5412 top-level block diagram and descriptions of the individual blocks.



#### Legend

The following list describes the individual blocks:

- Onboard Reference clock derives frequencies and sample rates when generating waveforms.
- Onboard Memory stores the waveform data and generation instructions that you load into the device.
- *Clocking* allows you to create your Sample clock and Reference clock.
- The Waveform Generation Engine retrieves the waveform data and instructions from the Onboard Memory using the Sample clock. The Waveform Generation Engine also uses this clock to retrieve triggers from Trigger and Event Control.
- The output from the *Waveform Generation Engine* is sent to the *DAC* device after any digital gain is applied.

- The *DAC* also contains an selectable *Digital Filter*, which interpolates and filters the waveform data.
- The waveform data is sent from the *DAC* to the *Analog Output path* where the waveform data is amplified.
- The *Routing Matrix* allows flexible routing of the RTSI trigger lines and the external PFI lines.

## NI PCI-5412/5421 Clock Source and Frequency

The NI 5412/5421 has a Sample clock rate of 10 Hz to 100 MHz. The timing of the NI 5412/5421 is very flexible, and you have multiple choices for deriving the Sample clock. There are modes for deriving the Sample clock from the internal Sample clock timebase, as well as modes to provide external clocks. You also have several choices for providing the frequency reference for the onboard phase-locked loop.



Note The male VHDCI (Digital Data & Control) connector is not available on the NI 5412 or the NI 5421/5422 with the 8 MB memory option.

## **Related Topics**

Sample Clock Sources - <u>NI 5412</u> or <u>NI 5421</u> <u>Internal Sample Clock Sources</u> <u>PLL Reference Sources</u> External Sample Clock Sources - <u>NI 5412</u> or <u>NI 5421</u> Exporting Clocks - <u>NI 5412</u> or <u>NI 5421</u>

# NI 5421 Overview

The NI 5421 is a 100 MS/s, 16-bit arbitrary waveform generator with the following features:

- One 16-bit resolution output channel
- Output amplitude up to 12  $V_{pk\text{-}pk}$  into a 50  $\Omega$  load
- Offset up to ±25% of V_{pk-pk}
- Up to 43 MHz sine output
- Up to 12.5 MHz square
- Up to 5 MHz triangle, ramp-up, and ramp-down
- Software-selectable output impedances (50  $\Omega$  or 75  $\Omega)$  and output attenuation levels from 0 dB to 51 dB
- High-Resolution, Divide by N, and external clocking
- PLL synchronization to external clocks or to PXI_CLK10
- NI-TClk support for multi-module synchronization. Refer to Start»All Programs»National Instruments»NI-TClk for more information.
- Sampling rate up to 100 MS/s
- Up to 256 MB of onboard waveform memory
- Waveform linking and looping for arbitrary waveform generation
- Digital and analog filters
- Digital gain
- Four external trigger inputs
- 4 Marker events as trigger output
- Optional 16-bit digital pattern generation with clock and LVDS
   output
- PXI trigger/RTSI lines

All NI 5421 devices follow industry-standard Plug and Play specifications for the PXI bus, and offer seamless integration with compliant systems.

## NI 5421/5422/5441 DIGITAL DATA & CONTROL Connector

The DIGITAL DATA & CONTROL (DDC) front panel connector is a 68-pin female VHDCI connector that contains the 16-bit LVDS digital pattern output. The DDC connector is an optional feature for the NI 5421/5422/5441.

# NI 5421/5422/5441 DIGITAL DATA & CONTROL Pin Assignments

The following figure shows the NI 5421/5422/5441 DDC 68-pin connector.



The following table lists the pin names and signal descriptions used for the NI 5421/5422/5441 DDC connector. All lines are at standard <u>LVDS</u> levels.

Signal Name	Туре	Description
D<015>	Output	Digital pattern outputs–The 16-bit digital representation of the analog waveform is available on

		these output pins as digital pattern outputs. This data is available directly from the memory after several Sample clock pipeline delays. The digital pattern outputs are standard LVDS output levels. All data bits change on the falling edge of the DDC CLK OUT.
DDC CLK IN	Input	Digital Data Clock In–These lines are used as a source for an external Sample clock. You can feed a LVDS level clock to this line with a maximum frequency of the signal generator.
DDC CLK OUT	Output	Digital Data Clock Out–The Sample clock is always routed to the DDC CLK OUT line of the DDC front panel connector when the digital pattern is enabled.
Ground	_	Digital ground
PFI<23> (Inputs)	Input	PFI<2:3>–These PFI lines can accept a trigger from an external source that can start or step through waveform generation. You can select this functionality on the NI 5421/5422/5441 through the software. Refer to <u>Trigger Sources</u> for more information.
PFI<4:5>	Output	<ul> <li>PFI&lt;45&gt;–These PFI lines can route out a signal from the following sources:</li> <li>Marker</li> <li>Out Start trigger</li> </ul>
Reserved	_	Reserved for future use. Do not connect signals to this line.
Refer to the <u>NI 5421</u> , <u>NI 5422</u> , or the <u>NI 5441</u> specifications for information about acceptable input signal characteristics to connect to the DDC lines, as well as the output signal characteristics.		

You must enable the DDC connector before the signals in this table are available for use, refer to <u>niFgen Configure Digital Patterning</u> VI or <u>niFgen_EnableDigitalPatterning</u> and <u>niFgen_DisableDigitalPatterning</u> function topics for more information.

# NI 5421/5422/5441/5442 Low-Voltage Differential Signaling (LVDS)

Low-voltage differential signaling (LVDS) is a low-noise, low-power, lowamplitude method for high-speed digital data transfer.

The following figure shows a diagram of a typical LVDS circuit.



As you can see in the previous figure, a current source at the driver provides approximately 3.5 mA of current. The direction of the current across the transmission line depends on whether the driver drives a logic high level or low level. When the current reaches the receiver, a 100  $\Omega$  terminating resistor connects the two ends of the differential transmission line to provide a return path for the current. In addition, a voltage of approximately 350 mV is established across the two input terminals of the receiver. The differential voltage at the receiver is either positive or negative, depending on the direction of the current. The receiver recognizes a positive voltage signal as a logic high level (1) and a negative voltage as a logic low level (0).

The electrical characteristics of an LVDS signal offers some performance improvements compared to single-ended standards. For example, since the received voltage is a differential between two signals, the voltage difference between the logic high level and low level state can be smaller, allowing for faster rise and fall times. Also, the differential transmission scheme is less susceptible to common-mode noise than single-ended transmission methods.

The LVDS standard defines the electrical aspects of this type of data

transmission. The standard defines driver and receiver characteristics only. However, the standard does not create protocol, interconnect, or connector definitions because these aspects are application specific.



**Note** Refer to the ANSI/TIA/EIA-644-A electrical characteristics standard, *Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits*, Revision A, 2001 edition for more information.

# NI PXI-5421 Block Diagram

This topic contains information about the NI PXI-5421 top-level block diagram and descriptions of the individual blocks.



#### Legend

Note If it is installed in any slot other than Slot 2 of the PXI chassis, the NI 5421 can receive a signal on the PXI_STAR line and can route a signal on the PXI_STAR line back to Slot 2 of the PXI chassis.

The following list describes the individual blocks:

- Onboard Memory stores the waveform data and generation instructions that you load into the device.
- *Clocking* allows you to create your Sample clock and Reference clock.
- The Waveform Generation Engine retrieves the waveform data and

instructions from the *Onboard Memory* using the Sample clock. The *Waveform Generation Engine* also uses this clock to retrieve triggers from *Trigger and Event Control*.

- The output from the *Waveform Generation Engine* is sent to the *DAC* device and the *DIGITAL DATA* & *CONTROL Connector* on the front panel after any digital gain is applied.
- The *DAC* also contains a selectable *Digital Filter*, which interpolates and filters the waveform data.
- The waveform data is sent from the *DAC* to the *Analog Output path* where the waveform data is filtered and amplified.
- The *Routing Matrix* allows flexible routing of the PXI Trigger lines (RTSI) and the external PFI lines.

## NI 5421/5422/5441 Analog Output

The following figure shows the NI 5421/5422/5441 Analog Output signal path.



#### Legend

NI 5421/5422/5441 Analog waveforms are generated as follows:

 The 16-bit digital waveform data from the Waveform Generation Engine or OSP is passed to a digital gain circuit and then highspeed DAC. This DAC also implements a portion of the Analog Output signal path attenuation with a range of 0 dB to 3 dB. Refer to the NI 5421, NI 5422, or the NI 5441 specifications for the exact resolution. You can adjust the amount of attenuation by configuring the Arbitrary Waveform Gain or Amplitude properties or the NIFGEN_ATTR_ARB_GAIN or NIFGEN_ATTR_FUNC_AMPLITUDE attributes. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting.

- 2. Following the DAC, the signal can take one of two paths: the Direct path or the Main path with High-Gain and Low-Gain amplifiers. NI-FGEN selects the Main path by default. To select the Direct path manually, refer to the <u>Analog Path</u> property or the <u>NIFGEN_ATTR_ANALOG_PATH</u> attribute.
  - a. The Direct path bypasses the Analog Filter, the attenuation sections, and the amplifiers. Taking the amplifiers out of the signal path yields an output signal with the lowest distortion and a flat frequency response. Use the Direct path for communication signals. The Direct path can provide a maximum of 1 V_{pk-pk} output into 50  $\Omega$  with no offset and a maximum of 3 dB attenuation. A signal taking the Direct path skips steps 3 through 5 and continues at step 6.
  - b. If the Low-Gain or High-Gain Amplifier path is selected, the signal passes through a switchable lowpass Analog Filter, attenuators, and amplifiers.
- 3. The signal then passes through a switchable lowpass Analog Filter to remove <u>Aliased Images</u>. You can select whether to include the Analog Filter in the Analog Output path using either the <u>niFgen Configure Analog Filter</u> VI or the <u>niFgen_EnableAnalogFilter</u> or <u>niFgen_DisableAnalogFilter</u> functions.
- 4. The signal then passes through the DC Offset Amplifier that adds the desired DC offset voltage. You can adjust the amount of DC offset added to the signal, up to one half the value of the NI-FGEN gain setting. Refer to either the <u>Arbitrary Waveform Offset</u> or <u>DC</u> <u>Offset</u> properties or the <u>NIFGEN_ATTR_ARB_OFFSET</u> or <u>NIFGEN_ATTR_FUNC_DC_OFFSET</u> attributes for more information.
- 5. The signal then passes through the Pre-Amp Attenuation section, a set of selectable solid-state attenuators that provide 0 dB to 12 dB of attenuation in 3 dB increments. You can adjust the amount of attenuation by adjusting the Arbitrary Waveform Gain property or the NIFGEN_ATTR_ARB_GAIN attribute. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting. Refer to either the <u>Arbitrary</u> <u>Waveform Gain</u> or <u>Amplitude</u> properties, or the <u>NIFGEN_ATTR_ARB_GAIN</u> or

NIFGEN_ATTR_FUNC_AMPLITUDE attributes for more information.

- 6. Following the Pre-Amp Attenuation section, the signal can take one of two paths: the High-Gain or Low-Gain Amplifier path. NI-FGEN automatically selects the best amplifier path between the High-Gain and Low-Gain amplifiers by default based on the gain or amplitude setting. Alternatively, you can set the signal path to remain constant regardless of the gain setting for applications requiring one path or the other. Refer to the <u>Analog Path</u> property or the <u>NIFGEN_ATTR_ANALOG_PATH</u> attribute for more information.
  - a. The High-Gain Amplifier path is used for waveform output voltages greater than  $\pm 1.0$  V into 50  $\Omega$ . The amplifier has a fixed gain and is included in the signal path to enable the AWG to provide the maximum V_{pk-pk}.
  - b. The Low-Gain Amplifier path is used for waveforms that have all output voltages equal to or smaller than  $\pm 1.0$  V into 50  $\Omega$ . The amplifier has a fixed gain.
- 7. The signal passes through the Post Amp Attenuation section, a set of two passive attenuators 12 dB and 24 dB. You can adjust the amount of attenuation by configuring either the either the Arbitrary Waveform Gain or Amplitude properties, or the NIFGEN ATTR ARB GAIN or NIFGEN ATTR FUNC AMPLITUDE attributes . NI-FGEN

calculates and sets the correct amount of attenuation required, corresponding to the gain setting.

- 8. The signal then passes through the Output Enable relay. When the Output Enable relay is disabled, ground is connected to the output through a 50  $\Omega$  or a 75  $\Omega$  resistor. Intentionally, waveform generation continues while the output enable relay is disabled. When the relay is enabled, the analog waveform is seen at the CH 0 connector. You can enable or disable the output of the analog waveform generator, refer to the <u>niFgen Output Enable</u> VI or the <u>niFgen_ConfigureOutputEnabled</u> function for more information.
- 9. The signal then passes through a 50  $\Omega/75 \Omega$  selector to the CH 0 connector. You can configure the output impedance of the

analog waveform generator, refer to the <u>niFgen Configure Output</u> <u>Impedance</u> VI or the <u>niFgen_ConfigureOutputImpedance</u> function.

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**Note** The NI 5421/5422/5441 uses mechanical relays to switch between the optional paths and sections in the Analog Output path. When you change a setting that results in a relay to switch, the bouncing of electromechanical relays on the NI 5421/5422/5441 distorts the output signal for about 10 ms.

# NI 5421/5422/5441 Waveform Amplitude Control

The NI 5421/5422/5441 uses both amplifiers and attenuators to achieve needed amplitude settings.

## **Output Paths and Amplifiers**

The following figure shows three different gain paths: the Direct path, the High-Gain Amplifier path, and the Low-Gain Amplifier path.

The Direct path provides the output of the main DAC to the CH 0 with the fewest electronic components in the path. There are no programmable amplifiers and no method of adding DC offset to the waveform. The Direct path can generate a maximum of 1 V_{pk-pk} at the CH 0 output into matched load impedance. The maximum gain setting for an Analog Output path configured to Direct path is 0.527. Gain is a unitless value. The Low-Gain Amplifier path has a 2 V_{pk-pk} amplifier and is used for waveforms that have all output voltages equal to or smaller than 2.0 V_{pk-pk} into matched load impedance. The High-Gain Amplifier path has a 12 V_{pk-pk} amplifier and is used for waveforms that not be used for waveforms that have all output voltages equal to or smaller than 2.0 V_{pk-pk} into matched load impedance. The High-Gain Amplifier path has a 12 V_{pk-pk} amplifier and is used for waveforms that have output voltages greater than 2.0 V_{pk-pk} into matched load impedance. The gains of the amplifiers are constant. NI-FGEN automatically selects by default between the high-gain and low-gain amplifiers, depending on the NI-FGEN gain setting. Refer to either the Arbitrary Waveform Gain or

<u>Amplitude</u> property, or the <u>NIFGEN_ATTR_ARB_GAIN</u> or <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u> attribute for more information.

You can configure the High-Gain or the Low-Gain Amplifiers to remain in the Analog Output path regardless of gain setting. Refer to the <u>Analog</u> <u>Path</u> property or the <u>NIFGEN_ATTR_ANALOG_PATH</u> attribute for more information. Configuring the Low-Gain Amplifier path to remain constant regardless of the gain setting affects the maximum output value allowable for that particular gain setting. The maximum gain setting for an Analog Output path configured to Low-Gain Amplifier path is 2.0. The maximum allowable gain setting with NI-FGEN automatically selecting the Gain Amplifier path is 12.0. Gain is a unitless value.

In addition, the DC Offset Amplifier for adding <u>DC offset</u> to the signal is in the High-Gain and Low-Gain Amplifier paths prior to the attenuators and amplifiers. The DC Offset Amplifier can be fine-tuned for adding offset to your signal. This fine-tuning of the main DC Offset Amplifier is performed by the Offset DAC.

## NI 5421/5422/5441 Attenuation

The Analog Output signal path has two passive attenuation sections. Pre-Amp Attenuation is prior to the High-Gain and Low-Gain Amplifier paths, and Post-Amp Attenuation is after the High-Gain and Low-Gain Amplifier paths. In addition, the main DAC provides 0 dB to 3 dB of signal attenuation. The amplitude control is implemented after the DAC. Attenuating the DAC output signal allows you to vary your signal amplitude and still maintain the dynamic range of the DAC. You do not lose any bits from the digital representation of the signal as does the method of controlling amplitude by using smaller data ranges of the DAC, sacrificing dynamic range. Passive attenuation by Pre-Amp and Post-Amp Attenuation is not available if the Direct path is selected.

For the Low-Gain Amplifier and the High-Gain Amplifier paths, maximum attenuation is 51 dB. For Direct path, maximum output attenuation is 3 dB. NI-FGEN automatically determines the correct value of attenuation in dB, and configures the attenuation based on the set gain. The minimum gain setting for an Analog Output path configured to Direct path is 0.354. The minimum gain setting for an Analog Output path configured to High-Gain Amplifier path is .01691. The minimum allowable gain setting with NI-FGEN automatically selecting the Low-Gain Amplifier path is .00282. Gain is a unitless value.

NI-FGEN calculates and sets the correct amount of attenuation required that corresponds to your NI-FGEN gain setting. The correct amount of attenuation is implemented in the Pre-Amp and Post-Amp Attenuation sections to best achieve the desired output signal amplitude. You can set the amount of gain with the <u>Arbitrary Waveform Gain</u> property or the <u>NIFGEN_ATTR_ARB_GAIN</u> attribute.

#### **Pre-Amp Attenuation**

The Pre-Amp Attenuation section is before the Low-Gain and High-Gain amplifiers. The attenuators provide a range of attenuation from 0 dB to a maximum of 12 dB in steps of 3 dB. NI-FGEN automatically controls the value of attenuation set in the Pre-Amp Attenuation section depending on the set gain.

Pre-Amp Attenuation improves the distortion of a signal because amplifiers provide lower distortion performance with smaller signals. However, attenuation lowers the amplitude of both the signal and the noise in a signal as the signal-to-noise ratio is unchanged upon attenuation. Amplifiers also have a fixed noise associated with them. The total noise at the amplifier output is obtained by taking the root of the sum of squares of the following factors:

- The input signal noise multiplied by the gain of the amplifier
- The amplifier noise

The total noise is dominated by the larger factor. If the signal is attenuated so that its noise when multiplied by gain at the amplifier input is smaller than the amplifier noise, then the output has a higher signal-tonoise ratio. This is a good reason to implement some of the AWG overall attenuation as Pre-Amp attenuation.

#### **Post-Amp Attenuation**

The Post-Amp Attenuation section is after the High-Gain and Low-Gain Amplifiers. The attenuators provide a range of attenuation from 0 dB to a maximum of 36 dB in steps of 12 dB. NI-FGEN automatically controls the value of attenuation set in the Post-Amp Attenuation section dependent on the set gain.

#### **DAC** Attenuation

The main DAC output can be fine-tuned for attenuation, which provides 0 dB to 3 dB of the Analog Output path signal attenuation. This finetuning of the main DAC attenuation is performed by the Gain DAC. The main DAC also provides the fine resolution for the attenuation settings.

#### **Summary of Gain Settings**

The following table summarizes the maximum and minimum gain setting that you can apply for the four NI-FGEN Analog path options. The default path is automatic. NI-FGEN automatically sets the path and correct amount of attenuation depending on the configured gain setting. These values assume a matched load impedance. Refer to the <u>NI 5421</u>, <u>NI 5422</u>, or the <u>NI 5441</u> specifications for more information about gain resolution.

NI 5421/5422/5441 Analog Path Gain Summary (matched load impedance)			
NI-FGEN Analog Path	Maximum Gain Value	Minimum Gain Value	

Automatic (default)	6.000	2.817 m
Direct	0.527	0.354
Fixed Low-Gain Amplifier	1.027	2.817 m
Fixed High-Gain Amplifier	6.000	16.91 m
Note: Gain is unitless.		

Note Digital gain is applied to the digital data before the data is passed to the DAC. Because relays are not used, digital gain allows glitch-free gain control at the expense of dynamic range.

## NI 5421/5422/5441 Output Impedance

The NI 5421/5422/5441 Analog Output path is designed to have an output impedance of 50  $\Omega$  from the Output Enable relay looking back towards the Main DAC. There is a selectable 25  $\Omega$  resistance that can be switched into the Analog Output path between the Output Enable Relay and the CH 0 SMB connector for applications requiring a 75  $\Omega$  impedance. Most applications use a load impedance of 50  $\Omega$ , but applications such as video testing, require 75  $\Omega$ . Refer to the following figure.



#### Legend

If the load impedance is a high impedance (~1 M $\Omega$ ), you may see output levels up to twice the selected output value for a matched input/output impedance. These levels can be as high as 24 V_{pk-pk} for the High-Gain Amplifier path. Normally, the output levels increase as the load impedance increases. The NI 5421/5422/5441 can compensate for different load impedance values. Refer to CH 0 Connector for more information.

You can select an output impedance of 50  $\Omega$  or 75  $\Omega$ . Refer to the <u>niFgen</u> <u>Configure Output Impedance</u> VI or the <u>niFgen_ConfigureOutputImpedance</u> function for more information.



**Note** The NI 5421/5422/5441 uses mechanical relays to switch between the 50  $\Omega$ /75  $\Omega$  switch states. When you change a setting that results in a relay to switch, the bouncing of electromechanical relays on the NI 5421/5422/5441 interrupts the output signal for up to 10 ms.

# NI 5421/5422/5441/5442 Sample Clock

Waveform generation is driven by the Sample clock; depending on your application, some sources may be better choices than others. You can use the following sources for the NI 5421/5422/5441/5442 Sample clock:

- Internal Sample clock—the Sample clock is derived from the Sample clock timebase via either Divide by N or High-Resolution clock mode.
- External Sample clock—the Sample clock is driven directly from an external source.
- Reference clock—the Sample clock is derived from an external source that is phase-locked to the Sample clock timebase.

The following table shows the valid NI-FGEN property or attribute value combinations that can be used to configure the

NI 5412/5421/5422/5441/5442 clock settings for an internal Sample clock, an external Sample clock, or a Reference clock. The term *Update clock* is synonymous with *Sample clock*.

Sample Clock Source [*]	Clock Mode*	PLL Reference Clock Source [*]
"OnboardClk" (default)	NIFGEN_VAL_DIVIDE_DOWN	"None"
		"PXI_CLK10", "RTSI7"
		"ClkIn", "RefIn"
		"OnboardRefClk"
	NIFGEN_VAL_HIGH_RESOLUTION	"None"
		"PXI_CLK10", "RTSI7"
		"ClkIn", "RefIn"
		"OnboardRefClk"
	NIFGEN_VAL_AUTOMATIC (default)	"None"
		"PXI_CLK10", "RTSI7"

1		I
		"ClkIn", "RefIn"
		"OnboardRefClk"
"ClkIn"	Not Applicable	Not Applicable
"PXI_STAR"		
"PXI_Trig<06>"		
"DDC_ClkIn"		
*These column he	adings refer to NI-FGEN p	roperties. The attributes
that correspond to	these properties are	
NIFGEN_ATTR_S	AMPLE_CLOCK_SOURCE,	
NIFGEN_ATTR_C	LOCK_MODE, and	
NIFGEN_ATTR_R	EFERENCE_CLOCK_SOUR	CE. The values in the
columns represen	t the values that can be set	on these properties or
attributes. Setting	s that line up horizontally sł	now valid combinations of
the NI-FGEN setti	ngs.	

## Sample Clock Source

The Sample clock source is the clock from which the Sample clock is derived, and it drives the DAC and all waveform generation operations on the device. You can set the Sample clock source by using the <u>Sample</u> <u>Clock Source</u> property or the <u>NIFGEN_ATTR_SAMPLE_CLOCK_SOURCE</u> attribute. The default NI-FGEN setting for the Sample Clock Source property or the NIFGEN_ATTR_SAMPLE_CLOCK_SOURCE attribute is "OnboardClk." The Sample clock source only requires configuration during applications that require an external Sample clock.

The NI 5421/5422/5441/5442 supports five options for the Sample clock source: one internal and four external sources. The fundamental clock source for your waveform generation application is the Sample clock timebase. The NI 5421/5441/5442 provides a high-precision 100 MHz voltage controlled crystal oscillator (VCXO) internal source from which all waveform generation operations are derived. The NI 5422 provides a high-precision 200 MHz VCXO internal source. The external sources are the NI 5421/5422/5441/5442 CLK IN front panel connector, DDC CLK IN on the DIGITAL DATA & CONTROL front panel connector (not available on the 5442), PXI_STAR, PXI_Trig<0..6> (PXI devices only), and the RTSI<0..6> (PCI devices only) lines.

For more information about configuring the Sample clock source for an external Sample clock, refer to <u>External Sample Clock Sources</u>.

## **Clock Mode**

The clock mode determines the method of deriving the Sample clock from the Sample clock timebase. You can set the clock mode with the <u>Clock Mode</u> property or the <u>NIFGEN_ATTR_CLOCK_MODE</u> attribute. The clock mode is only applicable when using an internal Sample clock.

There are three options for setting the clock mode on your NI 5421/5422/5441/5442: Divide-Down (Divide by N) Sampling, High-Resolution Sampling, and Automatic mode. The default NI-FGEN setting for the clock mode is Automatic. The Automatic mode setting switches between the Divide-Down and the High-Resolution mode depending on the sample rate configured with the <u>Sample Rate</u> property or the <u>NIFGEN_ATTR_ARB_SAMPLE_RATE</u> attribute.

For more information about configuring the clock mode, refer to <u>Internal</u> <u>Sample Clock Sources</u>.

## **PLL Reference Clock Source**

The phase-locked loop (PLL) Reference clock source specifies the source of the control voltage that tunes the VCXO of the Sample clock timebase for internal clock update sources. The PLL circuit adjusts the Sample clock timebase VCXO to synchronize to a Reference clock.

The frequency stability of the Sample clock timebase matches that of the PLL Reference clock when the two are phase-locked. Phase-locking also synchronizes multiple device clocks that are phase–locked to the same Reference clock.

You can set the PLL Reference clock source with the <u>Reference Clock</u> <u>Source</u> property or the <u>NIFGEN_ATTR_REFERENCE_CLOCK_SOURCE</u> attribute. There are five options for selecting the PLL Reference clock source on the NI 5421/5422/5441/5442: "None", "PXI_CLK10" (PXI), "RTSI7" (PCI), "OnboardRefClk" (PCI), and "ClkIn". The default NI-FGEN setting for the Reference Clock Source property or the NIFGEN_ATTR_REFERENCE_CLOCK_SOURCE attribute is "None".

For more information about the NI 5421/5422/5441/5442 PLL circuit, refer to <u>PLL Reference Sources</u>.

# NI 5421/5422/5441/5442 External Sample Clock Sources

The NI 5421/5422/5441/5442 can accept an external clock to directly drive the Sample clock. When using an external Sample clock, the frequency stability and accuracy of the Sample clock is determined by the provided external Sample clock.

The following figure shows the possible Sample Clock paths.



You have five options when choosing an external Sample clock to be the source of the Sample clock for the NI 5421/5422/5441/5442: the CLK IN front panel connector, DDC CLK IN on the NI 5421/5422/5441 DIGITAL DATA & CONTROL front panel connector (not available on the NI 5442), the PXI_STAR line or the PXI_Trig<0..6> lines on the PXI trigger bus, or the RTSI<0..6> lines.

Refer to <u>niFgen Configure Sample Clock Source</u> VI or the <u>niFgen_ConfigureSampleClockSource</u> function for more information about setting up the clock source.

The following table is a subset of the table in <u>Sample Clock Sources</u>, and shows the valid NI-FGEN property value combinations that can be used to configure the NI 5412/5421/5422/5441/5442 clock settings for an external Sample clock. The attributes that correspond to these properties

## are NIFGEN_ATTR_SAMPLE_CLOCK_SOURCE,

NIFGEN_ATTR_CLOCK_MODE, and

NIFGEN_ATTR_REFERENCE_CLOCK_SOURCE. The valid attribute value combinations will reflect the valid property combinations.

Sample Clock Source	Clock Mode	PLL Reference Clock Source
"ClkIn"	Not Applicable<	Not Applicable
"PXI_STAR"		
"PXI_Trig<06>"		
"DDC_ClkIn"		

You should configure the Sample clock rate when using an external Sample clock. Refer to the <u>niFgen Set Sample Rate</u> VI or the <u>niFgen_ConfigureSampleRate</u> function for more information about setting the Sample clock rate.



**Note** Refer to the <u>device specifications</u> for the allowable voltages, signal types, and clocks that you can use as an external Sample clock for all external Sample clocks.

## **External Sample Clock Considerations**

The NI 5421/5422/5441/5442 incorporates high-speed digital clocking technology and requires a stable, free-running Sample clock to operate properly. When the NI 5421/5422/5441/5442 is committed—either explicitly by calling the <u>niFgen Commit</u> VI or the <u>niFgen Commit</u> function or implicitly by writing waveforms or sequences or initiating a generation —the external Sample clock must be available to the device. If the external clock becomes unstable due to glitching, changing frequency, or is removed entirely, NI-FGEN returns a hardware clocking error.

Note If you are using NI 5441 or the NI 5442 with the OSP block enabled, refer to <u>Sample Clock Considerations</u> for more information about clocking while using onboard signal processing.

If necessary, you can change the rate or the source of the external Sample clock between subsequent generations by first calling the niFgen Abort Generation VI or the niFgen_AbortGeneration function, changing the rate or source, and then calling the niFgen Commit VI or the niFgen_Commit function. NI-FGEN reprograms the NI 5421/5422/5441/5442 for the new settings, and you can call the niFgen Initiate Generation VI or the niFgen_InitiateGeneration function to start the next generation.

If you must remove the external Sample clock between generations (after calling the niFgen Abort Generation VI or niFgen_AbortGeneration function, but before calling the niFgen Initiate VI or the niFgen_Init function), but are not changing the frequency or source of the external clock, you can choose one of the following options:

- Call the niFgen Initiate VI or the niFgen_Init function, which returns a hardware clocking error because the external Sample clock is gone, then clear the error and call the niFgen Initiate VI or the niFgen_Init function again-causing NI-FGEN to reprogram the hardware to use the external clock again.
- Force the device to be recommitted by changing some property or attribute to another value and then back to its original value. This action causes NI-FGEN to re-commit the settings to hardware, which would not happen otherwise because NI-FGEN would not know that the external Sample clock was gone.



**Caution** When configuring an external Sample clock, set the sample rate to the exact frequency you are using to avoid data errors. Refer to the <u>niFgen Set Sample Rate</u> VI or the <u>niFgen ConfigureSampleRate</u> function for more information about configuring the sample rate.
### NI 5421/5422/5441/5442 Exporting Clocks

The NI 5421/5422/5441/5442 provides two resources for exporting your clocks and multiple destinations for routing.



The following table shows the available clock signals that can be routed to devices external to the NI 5421/5422/5441/5442 and the destination options.

Clock to be Exported	Destination Options
Sample Clock	PFI <01> SMB connector
	PXI_Trig<06>, RTSI<06>>
	DDC CLK OUT
Sample Clock Timebase	PFI <01> SMB connector
	PXI_Trig<06>, RTSI<06>
	DDC CLK OUT
Reference Clock	PFI <01> SMB connector
	PXI_Trig<06>, RTSI<06>
Onboard Reference Clock	RTSI7

#### Sample Clock

For synchronization purposes, the NI 5421/5422/5441/5442 allows you to export your Sample clock so that other devices can have the same timing as the NI 5421/5422/5441/5442. The Sample clock can be routed to the PFI <0..1> front panel SMB connectors, PXI_Trig<0..6> lines on the PXI trigger bus, or the RTSI<0..6> lines. Additionally, the Sample clock has a direct route to the DDC CLK OUT line on the DIGITAL DATA & CONTROL connector on the front panel (not available on the NI 5442).

Additionally, the exported clock can be divided down by an integer value (no less than 2) before being exported to the PFI<0..1> SMB connectors, PXI_Trig<0..6> lines, or the RTSI<0..6> lines. Refer to the Exported Sample Clock Divisor property or the

<u>NIFGEN_ATTR_EXPORTED_SAMPLE_CLOCK_DIVISOR</u> attribute for more information about configuring the Sample clock divisor.

#### Sample Clock Timebase

For synchronization purposes, the NI 5421/5422/5441/5442 allows you to export your Sample clock timebase so that other devices can have the same timing as the signal generator. The Sample clock timebase can be routed to the PFI <0..1> SMB connectors on the front panel, the PXI_Trig<0..6> lines on the PXI trigger bus, or the RTSI<0..6> lines. Additionally, the Sample clock timebase has a direct route to the DDC CLK OUT line on the DIGITAL DATA & CONTROL connector on the front panel (not available on the NI 5442).

Additionally, the exported clock can be divided down by an integer value before being exported to the PFI<0..1> SMB connectors, the PXI_Trig<0..6> lines, or the RTSI<0..6> lines. Refer to Exported Sample Clock Timebase Divisor property or the <u>NIFGEN_ATTR_EXPORTED_SAMPLE_CLOCK_TIMEBASE_DIVISOR</u> attribute for more information about configuring the Sample clock divisor.

#### **Reference Clock**

For synchronization purposes, the NI 5421/5422/5441/5442 allows you to export your PLL Reference clock so that other devices can lock their clock sources to the same signal. Referring to the previous image, this clock is the actual clock that is configured for the

NI 5421/5422/5441/5442 phase-locked loop circuit to use as a reference. You configure a Reference clock as a PLL Reference clock source for the signal to be available for exporting. The Reference clock can be routed to the PFI<0..1> SMB connectors on the front panel, the PXI_Trig<0..6> lines on the PXI trigger bus, or the RTSI<0..6> lines.



**Note** Although NI-FGEN allows values for Reference clock frequency on the NI 5421/5422/5441/5442 from 1 MHz to 20 MHz in 1 MHz increments, the NI 5421/5422/5441/5442 specifications are only valid with Reference clock frequencies from 5 MHz to 20 MHz.

#### **Onboard Reference Clock**

The onboard Reference clock is a dedicated 10 MHz clock for PCI modules only. The onboard Reference clock can only be exported to RTSI7, for other devices to use and reimport as the Reference clock.



**Tip** By exporting the onboard Reference clock and then reimporting it, all devices (including the master) can use the same Reference clock.

#### **Destination Options**

The following sections define the destinations for exported clocks.

**DDC CLK OUT**—You can export the Sample clock to the DDC CLK OUT line on the DIGITAL DATA & CONTROL (DDC) connector (not available on the NI 5442). Exporting the clock from this connection allows for synchronous clocking of the DDC data. You must enable the DDC connector before using the Sample clock. Refer to the <u>niFgen Configure</u> <u>Digital Patterning</u> VI or the <u>niFgen_EnableDigitalPatterning</u> and <u>niFgen_DisableDigitalPatterning</u> functions for more information about enabling the DDC connector.

**PFI <0..1>**—The Sample clock and the Reference clock can be exported to the PFI 0 and PFI 1 SMB connectors on the front panel to synchronize external devices. You must configure the device to export the desired clock to the PFI SMB connectors.

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**Note** PFI 0 is optimized to have lower jitter than PFI 1 for exporting the Sample clock or the Reference clock.

**PXI_Trig<0..6>**—The Sample clock and the Reference clock can be exported to the PXI_Trig lines or RTSI lines. The PXI and PCI standards allow for devices to route signals to other devices in your PXI chassis to enhance device to device synchronization. Refer to the chassis documentation for specifications to ensure the reference signal is within tolerance. You must configure the device to export the desired clock to the PXI_Trig line or RTSI line. When exporting signals, the following lines are equivalent:

- PXI_Trig<0..6> = RTSI_<0..6>
- PXI_STAR

Refer to <u>niFgen Export Signal</u> VI or the <u>niFgen_ExportSignal</u> function for more information about configuring the destinations for the desired clock signal.

# **Script Mode**

Script mode allows you to use scripting to link and loop multiple waveforms in complex combinations.

Call the <u>niFgen Configure Output Mode</u> VI or the <u>niFgen_ConfigureOutputMode</u> function to switch to script mode.

Write all waveforms that are referenced in the script by calling the <u>niFgen</u> <u>Write Named Waveform</u> VI or one of the <u>niFgen Write Named Waveform</u> <u>Functions</u> and associate the proper names to them.

After your waveforms are written to your device, call the <u>niFgen Write</u> <u>Script</u> VI or the <u>niFgen_WriteScript</u> function to write the script(s) containing the generation instructions to be executed. Multiple scripts can exist simultaneously on your device. If you write multiple scripts to your device, you must select the one you wish to execute by setting the <u>Script to</u> <u>Generate</u> property or the <u>NIFGEN_ATTR_SCRIPT_TO_GENERATE</u> attribute. Call the <u>niFgen Initiate Generation</u> VI, or the <u>niFgen_InitiateGeneration</u> function to execute the selected script.

**Notes** Internally, the script stores physical device memory locations to refer to named waveforms. Thus, you must write all waveforms to the device *before* writing the script, or the device does not know where the waveform is located. The niFgen Initiate Generation VI or the niFgen_InitiateGeneration function produces an error if this rule is violated. If you delete waveforms and rewrite them, rewrite the script to update it with the new locations, even if the script text has not changed.

In some cases at high Sample clocks, your script may result in an underflow error. Underflow errors in a script can be created by waveform size, marker placement, and specific script instructions. To avoid underflow errors, refer to the minimum waveform size in your <u>device specifications</u>.

#### **Related Topics:**

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- <u>Scripts</u>
- <u>Common Scripting Use Cases</u>
- <u>Scripting Instructions</u>

### NI 5412/5421/5422/5441/5442 Generating Marker Events in Script Mode

In <u>script mode</u>, you can create up to four markers for each waveform. To create markers in script mode, refer to the *NI Script Editor Help*. Then use the <u>niFgen Export Signal</u> VI or the <u>niFgen_ExportSignal</u> function to export the marker signal.



**Note** When exporting markers in script mode, you must specify the marker using the **Signal Identifier** parameter of the niFgen Export Signal VI or the **signalIdentifier** parameter of the niFgen_ExportSignal function.

## NI PCI-5421 Theory of Operation

Expand this topic for information about the NI PCI-5421 theory of operation.

### NI PCI-5421 Block Diagram

This topic contains information about the NI PCI-5421 top-level block diagram and descriptions of the individual blocks.



#### **Legend**

Note You can drive the PXI_STAR line only if the signal generator is installed in Slot 2 of the PXI chassis.

The following list describes the individual blocks:

- Onboard Reference clock derives frequencies and sample rates when generating waveforms.
- Onboard Memory stores the waveform data and generation instructions that you load into the device.
- *Clocking* allows you to create your Sample clock and Reference clock.
- The Waveform Generation Engine retrieves the waveform data and

instructions from the *Onboard Memory* using the Sample clock. The *Waveform Generation Engine* also uses this clock to retrieve triggers from *Trigger and Event Control*.

- The output from the *Waveform Generation Engine* is sent to the *DAC* device and the *DIGITAL DATA* & *CONTROL Connector* on the front panel after any digital gain is applied.
- The *DAC* also contains an selectable *Digital Filter*, which interpolates and filters the waveform data.
- The waveform data is sent from the *DAC* to the *Analog Output path* where the waveform data is filtered and amplified.
- The *Routing Matrix* allows flexible routing of the RTSI trigger lines and the external PFI lines.

## NI 5422 Overview

The NI 5422 is a 200 MS/s, 16-bit arbitrary waveform generator with the following features:

- One 16-bit resolution output channel
- Output amplitude up to 12  $V_{pk-pk}$  into a 50  $\Omega$  load up to 80 MHz
- Offset up to ±full scale
- Up to 80 MHz sine output
- Up to 100 MHz square
- Up to 10 MHz triangle, ramp-up, and ramp-down
- Software-selectable output impedances (50  $\Omega$  or 75  $\Omega)$  and output attenuation levels from 0 dB to 51 dB
- High-Resolution, Divide by *N*, and external clocking
- PLL synchronization to external Reference clocks or to PXI_CLK10
- NI-TClk support for multi-module synchronization. Refer to **Start»All Programs»National Instruments»NI-TClk** for more information.
- Sampling rate up to 200 MS/s
- Up to 512 MB of onboard waveform memory
- Waveform linking and looping for arbitrary waveform generation
- Analog filtering
- Digital gain
- Four external trigger inputs
- 4 Marker events as trigger output
- Optional 16-bit digital pattern generation with clock and LVDS output
- PXI trigger lines

All NI 5422 devices follow industry-standard Plug and Play specifications for the PXI bus, and offer seamless integration with compliant systems.

### NI PXI-5422 Block Diagram

This topic contains information about the NI PXI-5422 top-level block diagram and descriptions of the individual blocks.



#### Legend

Note If it is installed in any slot other than Slot 2 of the PXI chassis, the NI 5422 can receive a signal on the PXI_STAR line and can route a signal on the PXI_STAR line back to Slot 2 of the PXI chassis.

The following list describes the individual blocks:

- Onboard Memory stores the waveform data and generation instructions that you load into the device.
- *Clocking* allows you to create your Sample clock and Reference clock.
- The Waveform Generation Engine retrieves the waveform data and

instructions from the *Onboard Memory* using the Sample clock. The *Waveform Generation Engine* also uses this clock to retrieve triggers from *Trigger and Event Control*.

- The output from the *Waveform Generation Engine* is sent to the *DAC* and the *DIGITAL DATA & CONTROL Connector* on the front panel after any digital gain is applied.
- The waveform data is sent from the *DAC* to the *Analog Output path* where the waveform data is filtered and amplified.
- The *Routing Matrix* allows flexible routing of the PXI Trigger lines (RTSI) and the external PFI lines.

### NI PXI/PCI-5422 Internal Sample Clock

The NI 5422 can derive a Sample clock from its main internal timing source—the Sample clock timebase. The signal generator provides a high-precision 200 MHz Voltage Controlled Crystal Oscillator (VCXO) clock source for the Sample clock timebase. As shown in the following figure, the Sample clock timebase frequency is tuned by an Internal Calibration DAC control voltage when the <u>Reference Clock Source</u> property or the <u>NIFGEN_ATTR_REFERENCE_CLOCK_SOURCE</u> attribute is set to "None". The Internal Calibration DAC, which is calibrated at the factory and which you can also calibrate, provides for the Sample clock timebase to maintain a high quality frequency source.



There are two methods, referred to as clock modes, for creating the Sample Clock: Divide-Down (Divide by *N*) Sampling and High-Resolution Sampling.

In Divide-Down Sampling mode, the Divide by *N* circuit uses the Sample clock timebase of 200 MHz to create the frequency available for use as the Sample clock. Divide-Down Sampling mode can generate any Sample clock frequency of 200 MHz/*N*, where *N* is any integer from 1 to 40. The Divide-Down Sample clock can run at 200 MHz, 100.0 MHz, 66.66 MHz, 50.0 MHz, 40.0 MHz, 33.332 MHz, and so on. The low frequency limit in Divide-Down Sampling mode is 5 MHz (200 MHz/40). Divide-Down Sampling mode provides a high-quality clock with the lowest jitter.

The High-Resolution Sampling mode also uses the Sample clock timebase at 200 MHz to generate a frequency from 5 MHz to 200 MHz. In addition, the High-Resolution mode uses direct digital synthesis to generate very fine resolution increments on the order of microhertz. Refer to the NI 5422 specifications for more information.

The following table, a subset of the table in <u>Sample Clock Sources</u>, shows the valid NI-FGEN property or attribute values and combinations to configure the NI 5422 clock settings for an internal Reference clock. Refer to <u>niFgen Configure Clock Mode</u> VI or <u>niFgen_ConfigureClockMode</u> function for more information about setting up the clock.

Sample Clock Source	Clock Mode	PLL Reference Clock Source
"OnboardClk"	NIFGEN_VAL_DIVIDE_DOWN	"None" (default)
(default)	NIFGEN_VAL_HIGH_RESOLUTION	
	NIFGEN_VAL_AUTOMATIC (default)	

You can specifically set the clock mode for either Divide-Down Sampling or High-Resolution Sampling. Alternatively, you can select Automatic mode, which has NI-FGEN switch between the Divide-Down Sampling and High-Resolution Sampling mode, depending on the configured Sample Rate. NI-FGEN chooses the Divide-Down Sampling mode if the configured frequency exactly matches one of the possible divide-down frequencies. If the configured frequency does not match one of the possible divide-down frequencies, the High-Resolution Sampling mode is selected to provide the Sample clock frequency.



**Note** The jitter of the High-Resolution clocking mode is frequency dependent. Refer to the <u>NI 5422</u> specifications for more information.

#### NI PXI/PCI-5431 Overview

The NI 5431 is a video signal generator with the following features:

- One 12-bit resolution output channel
- Up to 8 MHz sine and transistor-transistor logic (TTL) waveform
  output
- Up to 1 MHz square, triangle, ramp up, and ramp down, as well as DC and noise
- Software-selectable output impedances of 50  $\Omega$  and 75  $\Omega$  output attenuation levels from 0 dB to 73 dB
- Phase-locked loop (PLL) synchronization to external clocks
- Sampling rate up to 40 MS/s
- 8,000,000-sample onboard waveform memory
- Waveform linking and looping for arbitrary waveform generation
- Digital and analog filters
- Function generation implemented with 32-bit direct digital synthesis (DDS)
- External trigger input
- Marker as trigger output
- 16-bit digital pattern generation with clock
- Real-Time System Integration (RTSI) and PXI triggers

All NI 5431 signal generators follow industry-standard Plug and Play specifications on both PXI and PCI buses and offer seamless integration with compliant systems. If the application requires more than one channel of arbitrary waveform generation, you can synchronize multiple devices on all platforms using RTSI/PXI bus triggers on devices that use the RTSI/PXI bus or the digital trigger on the I/O connector.

## NI 5431 Front Panel Connectors

The following figure shows the front panel for the NI PXI-5431. The front panels for both the NI PXI-5431 and NI PCI-5431 contain three types of connectors: BNC, SMB, and 50-pin very high-density SCSI (VHDSCSI). The main waveform generates through the VIDEO OUT.



### NI PXI/PCI-5431 SYNC OUT

The SYNC OUT front panel connector is a TTL version of the sine waveform generated at the output. The signal from the pre-amplifier is sent to a comparator, where the signal is compared against a level set by the *level DAC*. The output of this comparator is sent to the SYNC connector through a hysteresis buffer and a 50  $\Omega$  series resistor to reverse terminate reflected pulses.

You can use the SYNC output as a very high-frequency resolution, software-programmable clock source for many applications. You also can vary the duty cycle of SYNC output dynamically by changing the output of the level DAC. The SYNC output does not work for other types of generated waveforms.



**Note** You can change the duty cycle of the SYNC output at any time during waveform generation.

## NI PXI/PCI-5431 DigiSync

DigiSync enables or disables the digital output data lines on the module

When you select enabled in DigiSync, the VI inserts four digital synchronization signals in order vertical sync (Vsync), horizontal sync (Hsync), composite sync (Csync), and field identification (Field ID) into the four least significant bits of the video data. The video data is created and/or saved as 16-bit data, but only 12 of these bits are used to generate the analog video signal. When you create the four digital synchronization signals, it does not affect the analog signal quality.



**Note** Refer to <u>NI PXI/PCI-5411/5431 (Video) Digital Pattern</u> <u>Connector</u> for more information about the location of these TTL signals on the digital output connector of the NI 5431.



**Note** Select enabled in DigiSync only if the application needs the four TTL video synchronization signals.

### NI PXI-5431 Theory of Operation

Expand this topic for information about the NI 5431 theory of operation.

### NI PXI/PCI-5431 System Block Diagram

The NI PXI/PCI-5431 composite video generator is a modified version of the NI 5411 arbitrary waveform generator and is an arbitrary waveform generator that replays downloaded video data. You can easily create the necessary video data by using the NI Video Software Toolkit that takes care of the needed calculations and driver functions especially developed to interface between the computer and the NI 5431.

In the following figure, the user interface is the NI Video Generator Wizard or LabVIEW software applications. You can use either application to generate video signals. The hardware driver is the NI-FGEN software, which sets up the NI 5431 that replays downloaded video data. The Compute Video Data occurs when the video generation software program, NI-VIDEO, is called to compute the data to be downloaded to the NI 5431. The Disk Save/Load represents the computer, which stores saved files generated from the User Interface and loads saved files to the NI 5431 and then generates the analog video signal on the Analog Video Output Connector.



## NI PXI/PCI-5431 Video Signal Generation

The NI PXI/PCI-5431 generates an analog video signal by converting a data array from digital to analog. This digital data array is downloaded to the NI 5431 onboard memory. The resolution of the data is 16-bit, even though only 12 bits are used to represent the analog signal (12-bit DAC).

The update rate of the DAC depends on the video format, as shown in the following table.

Video Format	Data Rate (MHz)	Total Samples/Line	Active Image Samples/Line	Total Line Duration	Active Line Duration
M- NTSC/ M- PAL	20.013986	1,272	1,044	63.556 μs	52.16 μs
All others	20.000000	1,280	1,040	64.000 μs	52.00 μs

#### NI 5431 Timing Information

When a bitmap image is converted to a video signal, the image pixels are extracted line-by-line, and the composite video signal is calculated based on the image pixel values. However, a normal bitmap image with an aspect ratio of 4:3 includes fewer pixels than needed to map, one-by-one, the calculated samples of a video line. For example, in M-NTSC, a typical bitmap image size is  $640 \times 480$ , which is 480 lines of 640 pixels (640 = 480 * 4 / 3), but the number of active image samples per line in the final video signal is 1,044.

To calculate 1,044 active video samples based on 640 image pixels, the software interpolates the image data using a linear interpolation algorithm. While this interpolation has very little visible effect on the resulting composite video image, it is still measurable. Therefore, if you use the active images to perform precision measurements, you must have an input bitmap image of exactly 1,044 x 480. The following table shows the different image size values to use depending on the actual video format.

Video Format	Total Active Lines	Square Pixels per Line	Active Video Samples/Line	Interpolation Ratio	Active Line Duration
M- NTSC/ M- PAL	480/486	640	1,044	1.63125	52.16 μs
All other formats	576	768	1,040	1.35417	52.00 μs

In the BMPs directory, you can find full-precision bitmap images in the  $1,044 \times 480$  folder (use with M-NTSC or M-PAL formats) or the  $1,040 \times 576$  folder (use with all other formats).

Make the same considerations for insertion test signals (ITS). To keep the full accuracy (avoiding automatic interpolation) of a test signal inserted in the image, such as the vertical blanking interval shown in <u>Gray Scale Image and Extracted Line Profile</u>, you must make sure that the used test line data arrays have the correct length, which is 1,044 samples for M-NTSC and M-PAL, and 1,040 samples for all other formats.

## NI PXI/PCI-5401/5411/5431 **Frequency Resolution and Lookup Memory in Standard Function Mode**

Direct digital synthesis-based waveform generation implements the Standard Function mode, which requires that you first load one cycle of the desired waveform into the lookup memory. The size of the direct digital synthesis lookup memory is 16,384 samples. Each sample is 16bits wide.



Note One cycle of the waveform loaded into the memory should be exactly equal to the size of the direct digital synthesis lookup memory.

 $F_c$  = Sample clock for the accumulator

Set the NI 5401/5411/5431 at  $F_c$  = 40 MHz.

 $F_a$  = desired frequency of the output signal

N = accumulator size in bits

Set the NI 5401/5411/5431 at N = 32.

FCW = frequency control word to load into the accumulator to generate  $F_a$ 

The frequency control word is calculated using the formula:

 $FCW = (2^N \times F_a) / F_c$ 

The frequency resolution is given by:

frequency resolution =  $F_c / 2^N = (40 \times 10^6) / 2^{32} = 9.31322 \text{ mHz}$ 

For example, if you need to generate a frequency of 10 MHz, then the *FCW* is  $(2^{32} \times 10^{6})/(40 \times 10^{6})$ , which equals 1,073,741,824. If you need to generate a frequency of 1 Hz, then the FCW is  $(2^{32} \times 1)/(40 \times 10^6)$ , which equals 107.



Note On the NI PXI/PCI-5401/5411, the maximum frequency of a sine wave you can generate reliably is limited to 16 MHz and, for the NI PXI/PCI-5431, it is limited to 8 MHz. Other waveforms, such as

square or triangular waves and the user-defined waveform, are limited to 1 MHz.

You can also generate user defined periodic waveforms using Direct Digital Synthesis mode. Generating user defined waveforms this way is very limited; you are restricted to a single waveform, and this waveform should be exactly equal to the size of the lookup memory (16,384 samples). Periodic waveforms such as sine waves, triangular waveforms produce the best results due to the lack of short parts of the signal deviating drastically in amplitude from the waveform.

Non periodic waveforms such as pulse waveform that has only 100 of the total 16,384 samples at 1.0, and the remaining at 0.0 produce mixed results, because not every sample is generated during waveform generation. The higher the set function frequency, the fewer of the waveform samples that are generated. The full waveform of 16,384 samples is considered one cycle, and a setting of 1 MHz for the waveform will only use 40 samples from the waveform because the internal clock is always running at 40 MS/s. These 40 samples are equally spaced, an average of 409.6 samples apart. The pulse of 100 samples can and will be easily skipped during the waveform generation, only seeing 0 volts at the output for a time. Depending on the DDS clocking, one sample in the pulse is generated for a momentary pulse in the output.

To update every sample of an arbitrary waveform in lookup memory at the maximum clock rate of 40 MHz, the software writes an FCW value of  $2^{(N-L)}$ , where *N* is the size of the accumulator and *L* is the number of address bits of lookup memory (*L* = 14 bits). Thus, the FCW value for the NI 5411/5431 equals 262,144. Because *FCW* =  $(2^N \times F_a) / F_c$ ,  $F_a = (2^{(N-L)} \times F_c) / 2^N$ , you write a frequency value of  $(2^{(32-14)} \times (40 \times 10^6)) / 2^{32}$ , which equals 2.441 kHz.

If you want to update every sample in lookup memory at an integral subdivision, D, of the maximum clock rate, then you want an FCW value of  $2^{(N-L-D+1)}$ . In other words, for an effective update rate of every sample at half the maximum clock rate, write a frequency value of  $(2^{(32-14-2+1)} \times (40 \times 10^6)) / 2^{32}$ , which equals 1.221 kHz.

#### NI PXI/PCI-5431 Calibration

Before shipping you the NI PXI/PCI-5431, NI calibrated your device to ensure that all features are within specifications.

Calibration is a set of operations that compares the values indicated by a measuring instrument or measuring system to the corresponding values realized by external standards. The result of calibration can be used to determine the measurement error and can correct for it in the adjustment process.

The calibration process consists of verifying, adjusting, and reverifying a device. During verification, you compare the measured performance to an external standard of known measurement uncertainty to confirm that the product meets or exceeds specifications. During adjustment, you correct the measurement error of the device by adjusting the calibration constants and storing the new calibration constants in the EEPROM. The host computer reads the calibration constants and the software uses them to compensate for errors in the data and to present calibrated data to the user.

For more information about calibrating NI signal generators, refer to <u>ni.com/calibration</u>.

## NI 5441 Overview

The NI 5441 is a 100 MS/s, 16-bit arbitrary waveform generator with the following features:

- Onboard signal processing (OSP)
- One 16-bit resolution output channel
- Output amplitude up to 12  $V_{pk-pk}$  into a 50  $\Omega$  load
- Offset up to ±25% of V_{pk-pk}
- Up to 43 MHz sine output
- Up to 25 MHz square
- Up to 5 MHz triangle, ramp-up, and ramp-down
- Software-selectable output impedances (50  $\Omega$  or 75  $\Omega)$  and output attenuation levels from 0 dB to 51 dB
- High-Resolution, Divide by N, and external clocking
- PLL synchronization to external clocks or to PXI_CLK10
- TClk synchronization
- Sampling rate up to 100 MS/s (105 MHz with external clock)
- Up to 512 MB of onboard waveform memory
- Waveform linking and looping for arbitrary waveform generation
- Digital and analog filters
- Digital gain
- Four external trigger inputs
- 4 Marker events as trigger output
- 16-bit digital pattern generation with clock and LVDS output
- PXI trigger lines

All NI 5441 devices follow industry-standard Plug and Play specifications for the PXI bus, and offer seamless integration with compliant systems.

### NI PXI-5441 Block Diagram

This topic contains information about the NI PXI-5441 top-level block diagram and descriptions of the individual blocks.



#### Legend

Note If it is installed in any slot other than Slot 2 of the PXI chassis, the NI 5441 can receive a signal on the PXI_STAR line and can route a signal on the PXI_STAR line back to Slot 2 of the PXI chassis.

The following list describes the individual blocks:

- Onboard Memory stores the waveform data and generation instructions that you load into the device.
- *Clocking* allows you to create your Sample clock and Reference clock.
- The *Waveform Generation Engine* retrieves the waveform data and instructions from the *Onboard Memory* using the Sample clock.

The Waveform Generation Engine also uses this clock to retrieve triggers from *Trigger and Event Control*.

- The output from the *Waveform Generation Engine* is sent to the *DAC* device and the *DIGITAL DATA & CONTROL Connector* on the front panel after any digital gain or onboard signal processing is applied.
- The *DAC* also contains a selectable *Digital Filter*, which interpolates and filters the waveform data.
- The waveform data is sent from the *DAC* to the *Analog Output path* where the waveform data is filtered and amplified.
- The *Routing Matrix* allows flexible routing of the PXI Trigger lines (RTSI) and the external PFI lines.

# **Onboard Signal Processing (OSP)**

The onboard signal processing (OSP) block is a general-purpose block of digital signal processing components that can be used to modify the data pulled from waveform memory during generation.

Common OSP block applications include:

- Arbitrary Waveform Generation
- Single-Tone
- Quadrature Upconversion
- Quadrature Upconversion with Signal Impairments
- Amplitude Modulation (AM)
- Baseband Interpolation

# **Onboard Signal Processing Components**

The following figure shows the block diagram of the OSP block.



The OSP block includes the following components:

- IQ Rate Component
- Pre-Filter Gain and Pre-Filter Offset
- FIR (Frequency Impulse Response)
- CIC (Cascaded Integrator Comb)
- <u>NCO (Numerically Controlled Oscillator)</u>
- IQ Combiner

## NI 5441 IQ Rate Component

The IQ rate component holds off the data from the output engine so that a new sample is only output once every Total_OSP_Interpolation Sample clocks where:

Total_OSP_Interpolation = FIR Interpolation × CIC Interpolation



**Note** The Total_OSP_Interpolation does not include the DAC interpolation.

NI-FGEN calculates the <u>FIR Interpolation</u>, <u>CIC Interpolation</u>, and the <u>Sample Rate</u> based on the specified <u>IQ Rate</u>.



**Tip** To override the FIR interpolation rate and/or CIC interpolation rate calculated by NI-FGEN, you can set the <u>FIR Interpolation</u> <u>Factor</u> and/or the <u>CIC Interpolation Factor</u> properties.

## NI 5441 Prefilter Gain and Offset

You can use the following prefiltering components to add impairments to your data and/or to eliminate overflows that occur later in the <u>OSP</u> block.

#### **Related Topics**

- Prefilter Gain
- Prefilter Offset

### NI 5441 Pre-Filter Gain

Pre-filter gain can be used to change the gain of the I and Q stream during signal generation. The I and Q pre-filter gains can be changed independently by setting the Pre-Filter Gain I and Pre-Filter Gain Q properties. The gain can range from -2.0 to +2.0 (unitless). Any time the pre-filter gain changes, the OSP block ignores all overflows for the next 50 IQ samples. If an overflow occurs during these 50 samples, the data is clipped but an error is not returned. Overflows are common during the first 50 IQ samples after a pre-filter gain change because the abrupt change is seen as a transient by the FIR filter. The pre-filter gain can be used to attenuate the IQ data in order to eliminate overflows in later stages of the OSP block. You can also use the pre-filter gain to <u>simulate IQ gain imbalance impairments</u>.

#### **Pre-Filter Gain Overflow**

Any time the following condition is not true for the I or Q data stream, an overflow occurs when pre-filter gain is applied:

 $-1 \leq \text{User Data} \times \text{Pre-Filter Gain} \leq 1$ 

If an overflow occurs, the data is clipped and NI-FGEN returns an error. To prevent data clipping, attenuate the waveform data or reduce the prefilter gain.



**Tip** To disable error reporting caused by OSP overflows, set the OSP Overflow Error Reporting property or the NIFGEN_ATTR_OSP_OVERFLOW_ERROR_REPORTING attribute.
#### NI 5441 Pre-Filter Offset

Pre-filter offset can be used to add offset to the I and Q stream during signal generation. The I and Q pre-filter offsets can be changed independently by setting the Pre-Filter Offset I and Pre-Filter Offset Q properties. The offset can range from negative Full Scale (-1) to positive Full Scale (+1). Any time the pre-filter offset changes, the OSP block ignores all overflows for the next 50 IQ samples. If an overflow occurs during these 50 samples, the data is clipped but an error is not returned. Overflows are common during the first 50 IQ samples after a pre-filter offset change because the abrupt change is seen as a transient by the FIR filter. You can use the pre-filter offset to simulate I/Q DC offset impairments.

#### **Pre-Filter Offset Overflow**

Any time the following condition is not true for the I or Q data stream, an overflow occurs when pre-filter offset is applied:

 $-1 \leq$  (User Data × Pre-Filter Gain) + Pre-Filter Offset  $\leq 1$ 

If an overflow occurs, the data is clipped and NI-FGEN returns an error. To prevent data clipping, reduce the <u>pre-filter gain</u>, attenuate the waveform data, or reduce the pre-filter offset.



**Tip** To disable error reporting caused by OSP overflows, set the OSP Overflow Error Reporting property or the <u>NIFGEN_ATTR_OSP_OVERFLOW_ERROR_REPORTING</u> attribute.

# **FIR Filter**

The Finite Impulse Response (FIR) filter shapes the incoming data and compensates for roll-off in the <u>CIC filter</u>. The I and Q FIR filters share the same set of coefficients. These coefficients must be <u>symmetric</u>. The FIR filters can be enabled/disabled by setting <u>FIR Filter Enabled</u> and <u>CIC Filter Enabled</u> properties.



**Note** The FIR and the CIC Filters must have the same enable/disable setting.

When using the FIR filter, consider the following:

- Interpolation
- Overflow
- FIR Filter Types

#### **Basic FIR Structure**

The following figure shows a diagram of a typical N-tap FIR filter:



The structure of the FIR filter is a long shift register. Each tap in the shift register is multiplied by an associated coefficient (c(x) in the figure above). The results for all of the taps are then summed to create the final output of the filter.

#### **Symmetric FIR filters**

The FIR filters in the OSP block are symmetric. This means that the first and last taps have the same coefficient, the second and second to last taps have the same coefficient, and so on. Because the FIR filter in the OSP has an odd number of taps, the center tap does not have a matching tap.

# **FIR Filter Interpolation**

The FIR filter is an interpolating filter. The interpolation options are 2x, 4x, and 8x.

The 2x interpolation option allows some aliasing in the spectrum which can create fairly significant spurs near the FIR output sample rate. The size of these spurs depend on the type of pulse shaping used in the FIR filter.

## **FIR Filter Overflow**

The FIR filter implementation in the OSP is designed for unity-gain. If the coefficients for the FIR are not scaled correctly, or there are transients in the input waveform to the FIR, then an overflow can occur. If such transients are expected, you should attenuate the data or adjust the prefilter gain so that the overflow does not occur. When the FIR overflows, the data is clipped at the rail where the overflow occurred and the OSP block continues to process data. NI-FGEN returns an error when the status of the signal generator is checked. NI-FGEN ignores all overflows for the first 50 IQ samples of a generation and for 50 samples after the pre-filter offset or pre-filter gain is changed. If an overflow occurs during these 50 samples, the data is clipped but an error is not returned. Overflows are common during the first 50 IQ samples of a generation because the filter is initialized with zeros. If the first point of generation is a full scale value, then this is seen as a transient step response by the FIR filter and an overflow can occur. Overflows are also common when the and <u>pre-filter offset</u> or <u>pre-filter gain</u> is changed during generation because sudden changes to the gain or offset are seen as transient step responses by the FIR filter.

Tip To disable error reporting caused by OSP overflows, set the OSP Overflow Error Reporting property or the <u>NIFGEN_ATTR_OSP_OVERFLOW_ERROR_REPORTING</u> attribute.

## NI 5441 FIR Filter Types

There are a number of built-in low-pass filters available in NI-FGEN. These filters compensate for the CIC roll-off and handle scaling issues. NI-FGEN calculates the coefficients for each filter which can then be queried with the <u>niFgen Get FIR Filter Coefficients</u> VI or the <u>niFgen_GetFIRFilterCoefficients</u> function. Because the coefficients are scaled for unity-gain, the filters may overflow if transients (such as step response) are presented at the input of the filter. Use the <u>Filter Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute to set the FIR filter type. The following filters are currently available:

- <u>Flat</u>
- <u>Raised Cosine</u>
- Root Raised Cosine

#### NI 5441 FIR Filter Type: Flat

Passband Values : 0.1 to 0.4

This low-pass filter is designed to give a flat response until the passband value. The passband value is a fraction of the <u>IQ Rate</u> coming into the FIR filter. Use the <u>Flat Filter Passband</u> property or the <u>NIFGEN ATTR OSP FIR FILTER FLAT PASSBAND</u> attribute to set the passband value.

**Caution** The Flat filter stopband does not begin until  $0.6 \times IQ$ Rate. If you provide data that has frequency content above  $0.4 \times IQ$  Rate, then aliasing occurs in the output spectrum. It is recommended to keep all frequency content below  $0.4 \times IQ$  Rate when using the Flat filter.

The following diagram shows the Flat Filter response with a passband of 0.4. The frequency axis is scaled as a fraction of the <u>IQ Rate</u>.



#### NI 5441 FIR Filter Type: Raised Cosine

Alpha Values: 0.1 to 0.9

This low-pass filter is commonly used in communications applications. The passband of the raised cosine filter stops at  $0.5 \times (1 - \alpha)$  of the IQ Rate. The stop-band of the raised cosine filter begins at  $0.5 \times (1 + \alpha)$  of the IQ Rate. The transition-band of the raised cosine filter (in dB) follows the following formula:

```
Ideal Raised Cosine Response(f) = 20\log_{10}\left(0.5 + 0.5\cos\left[\frac{\pi(f-S)}{\sigma}\right]\right)
```

where

 $S = 0.5 \times (1 - \alpha)$ 

f = Frequency (fraction of the IQ Rate)

Use the Raised Cosine Filter Alpha property or the NIFGEN ATTR OSP FIR FILTER RAISED COSINE ALPHA attribute to set the  $\alpha$  value.

The following diagram shows an ideal raised cosine filter response with an  $\alpha$  of 0.5. The frequency axis is scaled as a fraction of the <u>IQ Rate</u>.



The MER/EVM (measurement of modulation accuracy) and stopband

attenuation improve with a higher  $\alpha$ .

#### NI 5441 FIR Filter Type: Root Raised Cosine

Alpha Values: 0.1 to 0.9

This low-pass filter is commonly used in communications applications. The passband of the root raised cosine filter stops at  $0.5 \times (1 - \alpha)$  of the IQ Rate. The stop-band of the root raised cosine filter begins at  $0.5 \times (1 + \alpha)$  of the IQ Rate. The transition-band of the root raised cosine filter (in dB) follows the following formula:

Ideal Root Raised Cosine Response(f) =  $20 \log_{10} \sqrt{0.5 + 0.5 \cos\left[\frac{\pi (f-S)}{\pi}\right]}$ 

where

 $S = 0.5 \times (1 - \alpha)$ 

f = Frequency (fraction of the IQ Rate)

Use the Raised Cosine Filter Alpha property or the NIFGEN_ATTR_OSP_FIR_FILTER_RAISED_COSINE_ALPHA attribute to set the  $\alpha$  value.

The following diagram shows an ideal root raised cosine filter response with an  $\alpha$  of 0.5. The frequency axis is scaled as a fraction of the <u>IQ Rate</u>.



The MER/EVM (measurement of modulation accuracy) and stopband attenuation improve with a higher  $\alpha.$ 

### **FIR Filter Type: Gaussian**

BT Values: 0.1 to 0.9

This low pass filter is commonly used in communications applications. The Gaussian filter follows the following formula:

Ideal Gaussian Response(f) =  $20\log_{10}^{e}$ 

where

```
f = Frequency (fraction of the IQ Rate)
```

Use the <u>Gaussian Filter BT</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_GAUSSIAN_BT</u> attribute to set the BT value.

The following diagram shows an ideal Gaussian filter response with a BT of 0.3. The frequency axis is scaled as a fraction of the <u>IQ Rate</u>.



# **FIR Filter Type: Custom**

The custom filter lets you define the coefficients of the FIR filter.

#### **Custom Coefficients**

You can define the coefficients for the FIR filter and download them to the signal generator with the <u>niFgen Configure Custom FIR Filter Coefficients</u> VI or the <u>niFgen_ConfigureCustomFIRFilterCoefficients</u> function.

Coefficients should be <u>scaled</u> correctly and <u>compensate</u> for the <u>CIC Filter</u> roll-off. To use the coefficients you define, specify a custom filter by setting the <u>Filter Type</u> property or the

<u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute. The NI 5441 has 95 <u>symmetrical coefficients</u> defined for the FIR filter.

#### **FIR Coefficient Scaling**

The coefficients should be scaled between -1 and 1. NI-FGEN quantizes the floating point inputs and downloads them into the OSP block. The coerced coefficients can be queried with the <u>niFgen Get FIR Filter</u> <u>Coefficients</u> VI or the <u>niFgen GetFIRFilterCoefficients</u> function. When scaling the coefficients, consider that the FIR is architected for unity gain. This means that if a data set of all full-scale positive values is passed into the FIR and the sum of the coefficients is equal to 1, then positive full scale is output from the FIR. In general, the coefficients should be scaled as high as possible so that the FIR does not overflow the incoming data set and the coefficients are still within the range of -1 to 1.

#### **CIC Compensation in the FIR**

In order to flatten the OSP block in the passband, the FIR coefficients should compensate for the roll-off in the <u>CIC filter</u>. The frequency response (in dB) of the CIC follows the following formula:

CICFrequencyResponse(f) = 20log₁₀ 6 
$$\left(\frac{\sin(\pi f)}{R \times \sin(\frac{\pi f}{R})}\right)$$

where

R = CIC Interpolation Rate

f = Frequency (fraction of CIC input sample rate)

The first zero of the CIC filter is always at the same frequency as the output of the FIR filter. The FIR response should be peaked the same amount that the CIC rolls off in the passband of your FIR response. For example, the following diagram shows the desired response from the FIR with 4x interpolation.



But, the CIC has the following response:



The final response after the FIR (with CIC compensation) and CIC filters:



# **CIC** Filter

A CIC (Cascaded Integrator Comb) filter is designed to allow high levels of interpolation without high levels of computation. Most of the interpolation in the OSP block is done in the CIC filter. The interpolation range of the CIC filter is 6x to 256x. The CIC filter is a series of combs (differentiators) followed by a zero stuffer, followed by a series of integrators. The CIC filter in the OSP has six stages (six combs and six integrators). The CIC filter can be enabled/disabled by setting the <u>CIC</u> <u>Filter Enabled</u> and <u>FIR Filter Enabled</u> properties.

Note The FIR and the CIC Filters must have the same enable/disable setting.

When using the CIC filter, consider the following:

- Frequency Response
- <u>Gain</u>



## **CIC Frequency Response**

The frequency response (in dB) of the CIC follows the following formula:

```
CICFrequencyResponse(f) = 20\log_{10} | 6 \frac{\sin(\pi f)}{R \times \sin(\frac{\pi f}{R})}
```

where

R = CIC Interpolation Rate

f = Frequency (fraction of CIC input sample rate)

The following diagram shows the response of a six stage CIC filter with 8x interpolation.



Notice that the frequency response has a significant amount of roll-off in the passband. You must compensate for <u>CIC</u> roll-off in custom <u>FIR filters</u> in order to obtain an overall flat response.

# **CIC** Gain

The CIC gain is applied after the <u>CIC filter</u>. The CIC filter gain is used to compensate for attenuation in the <u>FIR filter</u> and CIC filter. NI-FGEN automatically calculates and applies this gain when an FIR filter type other than Custom is used. You can override the CIC filter gain by setting the <u>CIC Filter Gain</u> property or the

NIFGEN ATTR OSP CIC FILTER GAIN attribute. You should be careful when setting the CIC gain to prevent CIC overflows from occurring. The CIC gain range is from 1.0 to 16.0.

# **CIC Overflow**

A CIC overflow can occur if the CIC gain is set too high for the incoming data set. When the CIC overflows, the data is clipped at the rail where the overflow occurred and the OSP block continues to process data. NI-FGEN returns an error when the status of the signal generator is checked.

Tip To disable error reporting caused by OSP overflows, set the OSP Overflow Error Reporting property or the NIFGEN_ATTR_OSP_OVERFLOW_ERROR_REPORTING attribute.

### NI 5441 Numerically Controlled Oscillator (NCO)

The Numerically Controlled Oscillator (NCO) is a digital circuit that creates two cosine waves of the same frequency (the <u>carrier frequency</u>) with two independent phases. You can use the Carrier Frequency property or the <u>NIFGEN ATTR OSP CARRIER FREQUENCY</u> attribute to set the carrier frequency. The I phase cosine waveform is multiplied by the I signal path, and the Q phase cosine waveform is multiplied by the Q data path. The I and Q phases are programmable from -180° to 180° by setting the <u>Carrier Phase I</u> and <u>Carrier Phase Q</u> properties or the or the NIFGEN ATTR OSP CARRIER PHASE I or or the NIFGEN ATTR OSP CARRIER PHASE Q attributes. The Carrier Phase O property only applies when the Data Processing Mode property is set to Complex or the NIFGEN ATTR OSP DATA PROCESSING MODE attribute is set to NIFGEN VAL COMPLEX. Both the frequency and the phases can be updated during generation. For guadrature upconversion, set the I phase to 0° and Q phase to -90°. The Carrier Phase I/Q properties can be used to simulate guadrature skew impairments. Change the I or Q Carrier Phase by the required quadrature skew to simulate this impairment.

### NI 5441 IQ Combiner

When the <u>Data Processing Mode</u> property is set to Complex or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute is set to NIFGEN_VAL_COMPLEX, the I and Q data streams are combined after they are multiplied with the carriers. The IQ combiner is implemented as  $I_p - Q_p$ . The combiner block dictates that the following must be true at any given time during the generation or an overflow can occur:

 $-1 \le I_p Cos(\omega t + \Phi_I) - Q_p Cos(\omega t + \Phi_Q) \le 1$  if the carrier is enabled or

 $-1 \le (I_p - Q_p) \le 1$  if the carrier is disabled

where  $I_{p}$  and  $Q_{p}$  are the processed I and Q streams

**Tip** If the OSP block is configured for <u>quadrature upconversion</u>, and the <u>Carrier Phase I</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_PHASE_I</u> attribute is set to 0° and the <u>Carrier Phase Q</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_PHASE_Q</u> attribute is set to -90°, then the IQ combiner must follow the following formula  $(I_p^2 + Q_p^2 \le 1)$  or an overflow can occur.

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When an overflow occurs, the data is clipped at the rail where the overflow occurred and the OSP block continues to process data. NI-FGEN returns an error when the status of the signal generator is checked.



**Tip** To disable error reporting caused by OSP overflows, set the OSP Overflow Error Reporting property to Disabled.

# **Basic Onboard Signal Processing Properties**

The following properties must be configured before you can use the OSP block:

- OSP Enabled
- Data Processing Mode
- IQ Rate
- <u>Carrier Enabled</u>
- <u>Carrier Frequency</u>
- FIR Filter Type

# **OSP Enabled**

The <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute activates the functionality of the OSP block. To use any of the features in the OSP block, you must enable onboard signal processing by setting this property or attribute.

# **Data Processing Mode**

Data Processing mode determines whether the OSP block uses only the I signal path to generate waveforms or uses the I and Q signal paths to generate complex waveforms. If the Data Processing Mode property is set to Real or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute is set to NIFGEN_VAL_OSP_REAL then only the I signal path is used. If the Data Processing Mode property is set to Complex or the NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE attribute is set to NIFGEN_VAL_OSP_COMPLEX, both the I and Q signal paths are used. Complex waveform data should be downloaded to the signal generator using the <u>niFgen_WriteWaveformComplexf64</u> function.

### NI 5441 IQ Rate

IQ Rate defines the rate at which data is processed by the OSP block. If the <u>Data Processing Mode</u> property is set to Real or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute is set to NIFGEN_VAL_OSP_REAL, then it is the rate at which each sample from waveform memory is taken from memory and inserted into the OSP block. If the Data Processing Mode property is set to Complex NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE attribute is set to NIFGEN_VAL_OSP_COMPLEX, then it is the rate at which each complex sample is taken from memory and inserted into the OSP block.

The actual <u>sample rate</u> is calculated by NI-FGEN based on the IQ Rate. NI-FGEN calculates the <u>FIR Interpolation Factor</u> and <u>CIC Interpolation</u> <u>Factor</u> properties or the

NIFGEN_ATTR_OSP_FIR_FILTER_INTERPOLATION and NIFGEN_ATTR_OSP_CIC_FILTER_INTERPOLATION attributes unless you set them. The following formula describes the relationship between the IQ rate, FIR interpolation rate, CIC interpolation rate, and sample rate:

Sample Rate = IQ Rate × FIR Interpolation × CIC Interpolation

Note When the onboard signal processing is enabled by setting the <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute, you cannot set the <u>Sample Rate</u> property or the <u>NIFGEN_ATTR_ARB_SAMPLE_RATE</u> attribute.

#### NI 5441 Sample Clock Considerations

The performance of the signal generator that is using the OSP block can be significantly affected by the purity of its Sample clock. Sample clocks with high amounts of jitter or phase noise can create spurs in the signal generator's spectrum that are not present when a pure Sample clock is used. If the <u>Clock Mode</u> property or the <u>NIFGEN ATTR CLOCK MODE</u> attribute is set to NIFGEN VAL AUTOMATIC, NI-FGEN often selects High-Resolution clocking in order to achieve a specific IQ Rate. Because High-Resolution clocking has more jitter than Divide-By-N clocking, extra spurs may occur in the spectrum of the signal generator's output. If these spurs cannot be tolerated, then you can either use a pure external clock as the Sample clock of the signal generator, or you can use software resampling to change the IQ data to an IQ Rate that works with Divide-By-N clocking. If you are resampling, pulse shaping should be done in software and the Filter Type property should be set to Flat or the NIFGEN ATTR OSP FIR FILTER FLAT PASSBAND attribute should be set to NIFGEN VAL OSP FLAT.

## NI 5441 Using an External Clock with the OSP Block

Some applications may require lower jitter or phase noise than the onboard High-Resolution clock of the NI 5441. You can use an external clock source to achieve spectral purity at any arbitrary IQ Rate. To determine the frequency of the sample rate for the external clock source, complete the following steps for the NI 5441.

- 1. Set the <u>Sample Clock Source</u> property or the <u>NIFGEN_ATTR_SAMPLE_CLOCK_SOURCE</u> attribute to the external <u>clock source</u> you are using.
- 2. Set the <u>IQ Rate</u> property or the <u>NIFGEN_ATTR_OSP_IQ_RATE</u> attribute.
- 3. (Optional) Set the EM <u>FIR Interpolation Factor</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_INTERPOLATION</u> attribute.
- 4. (Optional) Set the <u>CIC Interpolation Factor</u> property or the <u>NIFGEN_ATTR_OSP_CIC_FILTER_INTERPOLATION</u> attribute.
- 5. Read the value of the <u>Sample Rate</u> property or the <u>NIFGEN_ATTR_ARB_SAMPLE_RATE</u> attribute.
- 6. Set the external clock source sample rate to the EM frequency of the Sample Rate property you just read.
- 7. Validate that the external Sample clock source is connected to the NI 5441 connector specified in the Sample Clock Source property or the NIFGEN_ATTR_SAMPLE_CLOCK_SOURCE attribute and generating a clock before you continue configuring the NI 5441.

For more information about using external clocks with the NI 5441, refer to <u>External Sample Clock Sources</u>.

#### NI 5441 Carrier Frequency

The carrier frequency determines the frequency of the cosine waves (both I and Q) exported from the NCO. You can use the <u>Carrier</u> <u>Frequency</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_FREQUENCY</u> attribute to set the carrier frequency. This frequency is programmable during signal generation.

For IQ Rates below the interpolation range of the OSP block, NI-FGEN selects a lower Sample clock rate in order to achieve the requested IQ Rate. Because the carrier cannot be more than 0.43 × Sample Rate, these lower sample rates translate to lower valid carrier rates. The largest carrier frequency that can be generated for a given IQ Rate with a maximum <u>CIC interpolation</u> of 256× can be calculated using the following formula:

Max Carrier Frequency = IQ Rate × 256 × FIR Interpolation × 0.43

The following table summarizes the maximum carrier frequency for all FIR interpolation factors.

FIR Interpolation Factor	Approximate Maximum Carrier Frequency
2	220 × IQ Rate
4	440 × IQ Rate
8	880 × IQ Rate

# NI 5441 FIR Filter Type

The FIR Filter type determines the spectral shaping of the data done in the <u>FIR filter</u>. Use the <u>FIR Filter Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute to set the FIR filter type. The following filter types are supported:

- Flat
- <u>Raised Cosine</u>
- Root Raised Cosine
- <u>Gaussian</u>
- <u>Custom</u>

# **Common Onboard Signal Processing Applications**

The OSP block is particularly useful for the following applications:

- <u>Arbitrary Waveform Generation</u>
- Single-Tone
- Quadrature Upconversion
- Amplitude Modulation (AM) or Double Sideband
- Baseband Interpolation

### NI 5441 Arbitrary Waveform Generation



For normal arbitrary waveform generation, disable onboard signal processing by setting the <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute.
# Single-Tone

Waveform Output Memory Engine		→ Digital Gain → DAC Interp. DAC
	Onboard Signal Processing NCO	

Use the <u>function generation mode</u> to generate a single-tone. During single-tone generation, the <u>NCO</u> is used to create the output signal.

## NI 5441 Quadrature Upconversion



In quadrature upconversion, you give the I and Q complex waveform data to the OSP block. This data is then pulse shaped, interpolated up to a high sample rate, and then upconverted to a programmable carrier frequency. For quadrature upconversion, complete the following steps.

- 1. Enable onboard signal processing by setting the <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute.
- 2. Specify the use of complex numbers for the waveform data by setting the <u>Data Processing Mode</u> property or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute.
- 3. Set the <u>IQ Rate</u> property or the <u>NIFGEN_ATTR_OSP_IQ_RATE</u> attribute.
- 4. Set the <u>FIR Filter Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute.
- 5. Set the corresponding filter parameter or download a <u>custom set</u> <u>of FIR filter coefficients</u>.
- 6. Enable the carrier by setting the <u>Carrier Enabled</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_ENABLED</u> attribute.
- 7. Set the <u>Carrier Frequency</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_FREQUENCY</u> attribute.
- 8. Download the complex waveform data to the signal generator.
- Note If the complex waveform data has transients, use the <u>Pre-</u> <u>Filter Gain</u> I and Q to attenuate your data and prevent clipping.

#### With Signal Impairments

Signal Impairments can be added to a quadrature upconverted signal on the fly. IQ Gain Imbalance impairments can be simulated by changing the I or Q Pre-Filter Gain. The following formula converts from IQ Gain Imbalance (dB, must be negative) to Pre-Filter Gain (only the I or Q Pre-Filter Gain should be changed).



**Note** When simulating an IQ gain imbalance, only the I or Q pre-filter gain should be changed.

Pre-Filter Gain = 10^(IQ Gain Imbalance / 20)

I/Q DC Offset impairments can be simulated by changing the I and Q Pre-Filter Offset. The following formula converts from I/Q DC Offset (%) to I/Q Pre-Filter Offset.

```
Pre-Filter Offset = (DcOffset / 100) × PreFilterGain
```

Quadrature Skew impairments can be simulated by changing the I or Q Carrier Phase. Change the I or Q Carrier Phase by the required Quadrature Skew to simulate this impairment.

# NI 5441 Amplitude Modulation (AM) or Double Sideband



You can generate an AM radio signal with the OSP block. To generate an AM signal, complete the following steps.

- 1. Enable onboard signal processing by setting the <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute.
- 2. Specify the use of real numbers for the waveform data by setting the <u>Data Processing Mode</u> property or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute.
- 3. Set the <u>IQ Rate</u> property or the <u>NIFGEN_ATTR_OSP_IQ_RATE</u> attribute to the sample rate of the baseband data.
- 4. Set the <u>Pre-Filter Gain I</u> property or the <u>NIFGEN_ATTR_OSP_PRE_FILTER_GAIN_I</u> attribute to 0.5.
- Set the <u>Pre-Filter Offset I</u> property or the <u>NIFGEN_ATTR_OSP_PRE_FILTER_OFFSET_I</u> attribute to 0.5. Steps 4 and 5 ensure that all interpolated data is positive when it is mixed with the carrier.
- 6. Enable the carrier by setting the <u>Carrier Enabled</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_ENABLED</u> attribute.
- 7. Set the <u>Carrier Frequency</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_FREQUENCY</u> attribute to the station frequency.
- 8. Specify a flat FIR filter by setting the <u>FIR Filter Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute.
- Set the <u>Flat Filter Passband</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_FLAT_PASSBAND</u> attribute to 0.4.
- 10. Download the waveform data to the signal generator.

# NI 5441 Baseband Interpolation



Baseband interpolation allows the OSP block to interpolate signals at a low sample rate up to a high sample rate. Arbitrary pulse shaping of the data can also be done in the FIR filter. For baseband interpolation, complete the following steps.

- 1. Enable onboard signal processing by setting the <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute.
- 2. Specify the use of real numbers for the waveform data by setting the <u>Data Processing Mode</u> property or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute.
- 3. Set the <u>IQ Rate</u> property or the <u>NIFGEN_ATTR_OSP_IQ_RATE</u> attribute to the low sample rate of the waveform data.
- 4. Set the <u>FIR Filter Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute.
- 5. Set the corresponding filter parameter or download a <u>custom set</u> <u>of FIR filter coefficients</u>.
- 6. Disable the carrier by setting the <u>Carrier Enabled</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_ENABLED</u> attribute.
- 7. Download the low sample rate waveform(s) to the signal generator.

## NI 5442 Overview

The NI 5442 is a 100 MS/s, 16-bit arbitrary waveform generator for the PXI Express platform with the following features:

- <u>Onboard signal processing</u> (OSP) with 40 MHz of digital upconverter bandwidth
- One 16-bit resolution output channel
- Output amplitude with a maximum of 2  $V_{pk-pk}$  into a 50  $\Omega$  load
- Offset up to ±25% of V_{pk-pk}
- Up to 43 MHz sine waveform output
- Up to 25 MHz square waveform output
- Up to 5 MHz triangle, ramp-up, and ramp-down waveform output
- Software-selectable output impedances (50 or 75  $\Omega)$  and output attenuation levels from 0 to 51 dB
- High-Resolution and Divide by *N* internal clocking modes, as well as external clocking options
- PLL synchronization to external clocks or to PXI_CLK10
- TClk synchronization
- Sample rate up to 100 MS/s (105 MHz with external clock)
- Up to 512 MB of onboard waveform memory
- Waveform linking and looping for arbitrary waveform generation
- Digital and analog filters
- Digital gain
- Four external trigger inputs
- Four Marker events as trigger output
- PXI trigger lines

All NI 5442 devices follow industry-standard Plug and Play specifications for the PXI Express bus and offer seamless integration with compliant systems.

### NI PXIe-5442 Front Panel

The following figure shows the NI PXIe-5442 front panel. This front panel has four SMB connectors.



The  $\underline{CH 0}$  SMB connector is the analog output terminal from which arbitrary waveforms are generated.

The <u>CLK IN</u> SMB connector provides the device with an external Reference or external Sample clock.

The <u>PFI 0 and PFI 1</u> SMB connectors are multidirectional connectors for a number of different signals.

## NI 5442 CH 0 Connector

The CH 0 connector is the analog waveform output terminal. The maximum output levels from this connector depend on the type of load termination. For example, if the module terminates into a 50  $\Omega$  load, the maximum output levels are ±1 V, while the maximum output levels are ±2 V when the module terminates into a high-impedance load (HiZ). This difference is illustrated in the following figure.



If the output terminates into any other load, the levels are defined by the following formula:

$$V_{out} = \pm [R_L / (R_L + R_O)] \times 2 \vee$$

where

Vout is the maximum peak output voltage level

 $R_1$  is the load impedance in ohms

 $R_{O}$  is the output impedance of the module in ohms

Note For loads less than 50  $\Omega$ , load impedance compensation supports only combinations of gain and load impedance that meet the previous V_{out} equation.

By default,  $R_O = 50 \Omega$ , but you can set the output impedance to 75  $\Omega$  in NI-FGEN. Refer to the <u>niFgen Configure Output Impedance</u> VI or the <u>niFgen_ConfigureOutputImpedance</u> function for more information about configuring the output impedance.

You can set the amplitude of the generated output signal in terms of peak voltage by setting the gain value. NI-FGEN calculates and sets the correct amount of attenuation required for the desired gain value. Refer to the <u>Arbitrary Waveform Gain</u> or <u>Amplitude</u> properties, or the

NIFGEN_ATTR_ARB_GAIN or NIFGEN_ATTR_FUNC_AMPLITUDE attributes for more information about configuring the output signal amplitude.

#### Load Impedance Compensation

The NI 5442 has the ability to configure the output signal amplitude based on a user-configured load impedance setting. This capability is desirable when you use the NI 5442 with loads that are between 0  $\Omega$  and a high impedance. Refer to the <u>device specifications</u> for information about the output impedance tolerance.

By default, NI-FGEN assumes that the load impedance is equal to the output impedance. If they do not match, you can change the load impedance value that NI-FGEN uses in its load impedance compensation algorithm. NI-FGEN takes the load impedance into account when setting the amplitude and provides the amplitude specified in the configured gain setting, eliminating the use of the voltage divider equation. NI-FGEN compensates to give the desired peak-to-peak voltage amplitude or arbitrary gain (relative to 1 V). Refer to the Load Impedance property or <u>NIFGEN ATTR LOAD IMPEDANCE</u> attribute for more information about load impedance.

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**Note** The voltage output levels are set in the software and are based upon a 50  $\Omega$  load termination (the default), or based on the user–specified load resistance.

For specifications about the waveform output signal, refer to the <u>device</u> <u>specifications</u>.

## NI 5442 Block Diagram

This topic contains information about the NI PXIe-5442 top-level block diagram and descriptions of the individual blocks.



#### Legend

Note If the device is installed in any slot other than system timing slot of the PXI Express chassis, the NI 5442 can can import clocks on the PXI_STAR line. However, PXI Express signal generators cannot import triggers or export clocks or triggers over the PXI_STAR line.

The following list describes the individual blocks:

- Onboard Memory stores the waveform data and generation instructions that you load into the device.
- *Clocking* allows you to create your Sample clock and Reference clock.
- The *Waveform Generation Engine* retrieves the waveform data and instructions from the *Onboard Memory* using the Sample clock. The *Waveform Generation Engine* also uses this clock to retrieve

triggers from *Trigger and Event Control*.

- The output from the *Waveform Generation Engine* is sent to the *DAC* device after any digital gain or onboard signal processing is applied.
- The *DAC* also contains a selectable *Digital Filter*, which interpolates and filters the waveform data.
- The waveform data is sent from the *DAC* to the *Analog Output path* where the waveform data is filtered and amplified.
- The *Routing Matrix* allows flexible routing of the PXI Trigger lines and the external PFI lines.

#### NI 5442 Analog Output Path

The following figure shows the NI 5442 Analog Output path.



#### Legend

NI 5442 Analog waveforms are generated as follows:

- 1. The 16-bit digital waveform data from the waveform generation engine or OSP is passed to a digital gain circuit and then a highspeed DAC. This DAC also implements a portion of the Analog Output path attenuation with a range of 0 to 3 dB. Refer to the NI 5442 specifications for the exact resolution. You can adjust the amount of attenuation by configuring the <u>Arbitrary Waveform Gain</u> or <u>Amplitude</u> properties or the <u>NIFGEN_ATTR_ARB_GAIN</u> or <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u> attributes. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting.
- 2. Following the DAC, the signal can take one of two paths: the Direct path or the Main path. NI-FGEN selects the Main path by

default. To select the Direct path, refer to the <u>Analog Path</u> property or the <u>NIFGEN_ATTR_ANALOG_PATH</u> attribute.

- a. The Direct path bypasses the analog filter, the attenuation sections, and the amplifiers. Taking the amplifiers out of the signal path yields an output signal with the lowest distortion and a flat frequency response. Use the Direct path for communication signals. The Direct path can provide a maximum of 1  $V_{pk-pk}$  output into 50  $\Omega$  with no offset and a maximum of 3 dB attenuation. A signal taking the Direct path skips steps 3 through 5 and continues at step 6.
- b. If the Main path is selected, the signal passes through a switchable lowpass analog filter, attenuators, and amplifiers.
- 3. The signal then passes through a switchable lowpass analog filter to remove <u>aliased images</u>. You can select whether to include the analog filter in the Analog Output path using either the <u>niFgen</u> <u>Configure Analog Filter</u> VI or the <u>niFgen_EnableAnalogFilter</u> or <u>niFgen_DisableAnalogFilter</u> functions.
- 4. The signal then passes through the DC offset amplifier that adds the desired DC offset voltage. You can adjust the amount of DC offset added to the signal, up to half the value of the NI-FGEN gain setting. Refer to either the <u>Arbitrary Waveform Offset</u> or <u>DC</u> <u>Offset</u> properties or the <u>NIFGEN_ATTR_ARB_OFFSET</u> or <u>NIFGEN_ATTR_FUNC_DC_OFFSET</u> attributes for more information about configuring the offset.
- 5. The signal then passes through the preamplifier attenuation section, a set of selectable solid-state attenuators that provide 0 to 12 dB of attenuation in 3 dB increments. You can adjust the amount of attenuation by adjusting the Arbitrary Waveform Gain property or the NIFGEN_ATTR_ARB_GAIN attribute. NI-FGEN calculates and sets the correct amount of attenuation required, corresponding to the gain setting. Refer to either the Arbitrary Waveform Gain or Amplitude properties or the NIFGEN_ATTR_ARB_GAIN or NIFGEN_ATTR_FUNC_AMPLITUDE attributes for more information about configuring the gain.

- 6. Following the preamplifier attenuation section, the signal passes through an amplifier with a fixed gain.
- 7. The signal passes through the postamplifier attenuation section, a set of two passive attenuators 12 dB and 24 dB. You can adjust the amount of attenuation by configuring either the either the <u>Arbitrary Waveform Gain</u> or <u>Amplitude</u> properties or the <u>NIFGEN_ATTR_ARB_GAIN</u> or <u>NIFGEN_ATTR_FUNC_AMPLITUDE</u> attributes . NI-FGEN calculates and sets the correct amount of attenuation required for the current gain setting.
- 8. The signal then passes through the Output Enable relay. When the Output Enable relay is disabled, ground is connected to the output through a 50 or a 75  $\Omega$  resistor. Waveform generation continues while the Output Enable relay is disabled. The analog waveform is seen at the CH 0 connector when the relay is enabled. You can enable or disable the output of the analog waveform generator by using the <u>niFgen Output Enable</u> VI or the <u>niFgen_ConfigureOutputEnabled</u> function.
- 9. The signal then passes through a 50  $\Omega/75 \Omega$  selector to the CH 0 connector. You can configure the output impedance of the analog waveform generator by using the <u>niFgen Configure Output</u> <u>Impedance</u> VI or the <u>niFgen ConfigureOutputImpedance</u> function.
- Note The NI 5442 uses mechanical relays to switch between the optional paths and sections in the Analog Output path. When you change a setting that causes a relay to switch, the bouncing of electromechanical relays on the NI 5442 distorts the output signal for about 10 ms.

#### NI 5442 Waveform Amplitude Control

The NI 5442 uses both amplifiers and attenuators to achieve needed amplitude settings.

#### **Output Paths and Amplifiers**

The following figure shows two different gain paths: the Direct path and the Main path.

The Direct path provides the output of the main DAC to the CH 0 with the fewest electronic components in the path. There are no programmable amplifiers and no method for adding DC offset to the waveform. The Direct path can generate a maximum of 1 V_{pk-pk} at the CH 0 output into matched load impedance. The maximum gain setting for an Analog Output path configured to the Direct path is 0.527 (gain is a unitless value).

The Main path has a 2  $V_{pk-pk}$  amplifier and is used for waveforms that have all output voltages equal to or smaller than 2.0  $V_{pk-pk}$  into matched load impedance. Refer to either the <u>Arbitrary Waveform Gain</u> or <u>Amplitude</u> property or the <u>NIFGEN ATTR ARB GAIN</u> or <u>NIFGEN ATTR FUNC AMPLITUDE</u> attribute for more information about configuring the gain.

In addition, the DC offset amplifier, which adds <u>DC offset</u> to the signal, is located in the High-Gain and Low-Gain Amplifier paths prior to the attenuators and amplifiers. The DC offset amplifier can be fine-tuned to add offset to your signal. This fine-tuning of the main DC offset amplifier is performed by the offset DAC.

#### NI 5442 Attenuation

The Analog Output path has two passive attenuation sections. Preamplifier attenuation is prior to the amplifier, and postamplifier attenuation is after the amplifier. In addition, the main DAC provides 0 to 3 dB of signal attenuation. The amplitude control is implemented after the DAC. Attenuating the DAC output signal allows you to vary your signal amplitude and while maintaining the dynamic range of the DAC. You do not lose any bits from the digital representation of the signal as does the method of controlling amplitude by using smaller data ranges of the DAC, sacrificing dynamic range. Passive attenuation by pre-amplifier and postamplifier attenuation is not available if the Direct path is selected.

For the Main path, maximum attenuation is 51 dB. For the Direct path, maximum output attenuation is 3 dB. NI-FGEN automatically determines the correct value of attenuation in dB and configures the attenuation based on the set gain. The minimum gain setting for the Direct path is 0.354. The minimum allowable gain setting with NI-FGEN automatically selecting the Main path is .00282 (gain is a unitless value).

NI-FGEN calculates and sets the correct amount of attenuation required that corresponds to your NI-FGEN gain setting. The correct amount of attenuation is implemented in the preamplifier and postamplifier attenuation blocks to best achieve the desired output signal amplitude. You can set the amount of gain with the Arbitrary Waveform Gain property or the NIFGEN_ATTR_ARB_GAIN attribute.

#### **Pre-Amplifier Attenuation**

The preamplifier attenuation section is located before the amplifier in the Main path. The attenuators provide a range of attenuation from 0 to a maximum of 12 dB in steps of 3 dB. NI-FGEN automatically controls the value of attenuation set in the preamplifier attenuation section depending on the set gain.

Preamplifier attenuation improves the signal distortion because amplifiers provide lower distortion performance with smaller signals. However, attenuation lowers the amplitude of both the signal and the noise in a signal as the signal-to-noise ratio (SNR) is unchanged upon attenuation. Amplifiers also have a fixed noise associated with them. The total noise at the amplifier output is obtained by taking the root of the sum of squares of the following factors:

- The input signal noise multiplied by the gain of the amplifier
- The amplifier noise

The total noise is dominated by the larger factor. If the signal is attenuated so that its noise when multiplied by gain at the amplifier input is smaller than the amplifier noise, then the output has a higher SNR. This higher SNR is a good reason to implement some of the AWG overall attenuation as preamplifier attenuation.

#### **Post-Amp Attenuation**

The post-amplifier attenuation section is located after the amplifier in the Main path. The attenuators provide a range of attenuation from 0 dB to a maximum of 36 dB in steps of 12 dB. NI-FGEN automatically controls the value of attenuation set in the postamplifier attenuation section dependent on the set gain.

#### **DAC** Attenuation

The main DAC output can be fine-tuned for attenuation, which provides 0 to 3 dB of the Analog Output path signal attenuation. This fine-tuning of the main DAC attenuation is performed by the Gain DAC. The main DAC also provides the fine resolution for the attenuation settings.

#### Summary of Gain Settings

The following table summarizes the maximum and minimum gain setting that you can apply for the NI-FGEN Analog path options. Refer to the NI 5442 specifications for more information about gain resolution.

NI 5442 Analog Path Gain Summary (Matched Load Impedance)				
NI-FGEN Analog Path	Maximum Gain Value	Minimum Gain Value		
Main Path (default)	1.027	2.817 m		
Direct Path	0.527	0.354		
Note: Gain is unitless				

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N **Note** Digital gain is applied to the digital data before the data is passed to the DAC. Because relays are not used, digital gain allows glitch-free gain control at the expense of dynamic range.

### NI 5442 DC Offset

The NI 5442 supports a DC offset before the attenuation chain that affects the maximum value of DC offset for a given gain setting. This preattenuation architecture requires two rules for setting the DC offset:

- 1. The magnitude of the maximum value of offset can be no more than  $\frac{1}{2}$  of the configured gain setting for the NI 5442.
- 2. The waveform maximum plus the offset must not exceed  $\pm 1$  V into 50  $\Omega$ ; if it does, the waveform is clipped.

For example, if you have set a gain of .75, which corresponds to an amplitude of .75  $V_{pk}$ , and the waveform is a sine wave using the full range of the DAC, the maximum DC offset you can apply without clipping the sine wave is ±.25 V. At this point, output voltages of the sine waveform have reached the maximum amplitude that the device supports. If you increase the DC offset further, the top portion of the waveform at 1 V is clipped.

NI-FGEN automatically calculates the preattenuation offset value based on the set DC offset and gain values. You can change the DC offset at any time during waveform generation. Refer to the <u>Arbitrary Waveform</u> <u>Offset</u> property or the <u>NIFGEN_ATTR_ARB_OFFSET</u> attribute for more information about setting the DC offset.

You cannot set the DC offset if you selected the Direct path. However, the output signal still has some non zero offset. Refer to the <u>NI 5442</u> <u>specifications</u> for information about the maximum value of the DC offset.

## NI 5442 Filtering Effects

The delay from the time at which a device receives a trigger to the time at which the analog output signal is generated increases if the digital and/or analog filters in the Analog Output path are enabled. In the case of digital filtering, delay also increases with increases in interpolation. Enabling the <u>onboard signal processing block</u> can also introduce delay.



**Note** The digital filter for the signal generator is inside the main DAC shown in the Analog Output path.

Refer to <u>Digital Filter</u> for interpolation options. Refer to the <u>NI 5442</u> <u>Specifications</u> for the delay from the time at which a device receives a trigger to the time at which the analog output signal is generated based on different filtering options.

## NI 5442 Digital Filter

The main DAC provides an internal digital filter. When digital filtering is enabled, the main DAC runs at a faster rate, referred to as the effective sample rate (ESR). The waveform data transfers to the main DAC at the configured Sample clock rate; the internal digital filter interpolates by a factor of 2x, 4x, or 8x; and the DAC generates the data at the ESR.

Effective sample rate is calculated with the following formula:

 $ESR = I_{fac} \times SR$ 

where

ESR = the Effective Sample Rate (MS/s)

 $I_{fac}$  = the interpolation factor

SR = configured Sample clock rate (MS/s)

The ESR applies only when the digital filter is enabled. The maximum ESR is 400 MS/s. The ESR is recommended to be as high as possible without exceeding 400 MS/s. The following table lists the allowed update and interpolation rates.



**Note** When the <u>OSP block</u> is enabled, you cannot set the <u>Sample</u> <u>Rate</u> property or the <u>NIFGEN_ATTR_ARB_SAMPLE_RATE</u> attribute. After you have configured the <u>IQ Rate</u>, you can read the sample rate.

<b>Recommended Interpolation Settings</b>			
Sample Clock Rate (MS/s)*	Interpolation		
12.5 to 105	2x		
10 to 100	4x		
10 to 50	8x		

Notes The digital filter is not available for use for Sample clock rates below 10 MS/s.

In Standard Function mode, the digital filter is enabled and disabled by NI-FGEN except when generating user-defined waveforms.

The delay from the time that the device receives a Start trigger to the time that the analog output signal is generated increases if the digital filter is enabled. The delay increases with an increase in the interpolation factor. Refer to the <u>device specifications</u> for information about the delay from the trigger to the analog output based on the configured filter settings.

In general, use the digital filter for signals containing large sinusoidal waveform content, such as AM and FM, sinc pulse, and sinusoidal chirp waveforms. The filter can be disabled for signals that are better represented without filtering, such as square waves or waveforms containing many pulse characteristics. If you enable the digital filter without setting the interpolation factor, NI-FGEN automatically uses the highest interpolation factor possible in accordance with the preceding table. Refer to the Configure Digital Filter VI or the niFgen_EnableDigitalFilter and niFgen_DisableDigitalFilter functions for more information about setting the digital filter.

Note NI recommends that you always enable or disable the analog filter (if available) and digital filter at the same time.

#### **Related Topics**

Filtering and Interpolation Aliased Images

## NI 5442 Output Enable

You can disable the analog output signal at the CH 0 connector by controlling the output enable relay, as shown in the following figure.



When the Output Enable relay is disabled, the output signal is connected to ground through a 50 or 75  $\Omega$  resistance depending on the output impedance selected. The Output Enable relay is enabled for normal waveform generation, connecting the CH 0 SMB connector to <u>Analog</u> <u>Output path</u>. You can change the output enable state at any time during waveform generation, and the generation continues on internally.

Refer to the <u>niFgen Output Enable</u> VI or the <u>niFgen_ConfigureOutputEnabled</u> function for more information about enabling the output.

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**Note** The signal generator uses mechanical relays to switch between the output enable states. When you change a setting that causes a relay to switch, electromechanical relay bouncing interrupts the output signal for up to 10 ms.

## NI 5442 Output Impedance

The NI 5442 Analog Output path is designed for an output impedance of 50  $\Omega$  from the Output Enable relay relative to the main DAC. A selectable 25  $\Omega$  resistance can be switched into the Analog Output path between the Output Enable relay and the CH 0 SMB connector for applications such as video testing that require a 75  $\Omega$  impedance. Refer to the following figure for more information about the operation and location of the output of the Output Enable relay.



#### Legend

If the load impedance is high (~1 M $\Omega$ ), you may see output levels up to twice the selected output value for a matched input/output impedance. These levels can be as high as 4 V_{pk-pk} for the Main path. Normally, the output levels increase as the load impedance increases. The NI 5442 can compensate for different load impedance values. Refer to <u>CH</u> <u>0 Connector</u> for more information on the output at the CH 0 connector.

You can select an output impedance of 50 or 75  $\Omega$ . Refer to the <u>niFgen</u> <u>Configure Output Impedance</u> VI or the <u>niFgen_ConfigureOutputImpedance</u> function for more information about setting the output impedance.

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Note The NI 5442 uses mechanical relays to switch between the 50 and 75  $\Omega$  output impedance states. When you change a setting that causes a relay to switch, electromechanical relay bouncing on the NI 5442 interrupts the output signal for up to 10 ms.

# **Onboard Signal Processing (OSP)**

The onboard signal processing (OSP) block is a general-purpose block of digital signal processing components that can be used to modify the data pulled from waveform memory during generation.

The OSP block can be used for the following common applications:

- <u>Arbitrary Waveform Generation</u>
- Single-Tone Generation
- Quadrature Upconversion
- Quadrature Upconversion with Signal Impairments
- Amplitude Modulation (AM)
- Baseband Interpolation

# **Onboard Signal Processing Components**

The following figure shows the block diagram of the OSP block.



The OSP block includes the following components:

- IQ Rate Component
- Prefilter Gain and Prefilter Offset
- Filtering and Interpolation
- <u>NCO (Numerically Controlled Oscillator)</u>
- IQ Combiner

## NI 5442 IQ Rate Component

The IQ rate component controls the data from the output engine so that a new sample is only generated once every Total_OSP_Interpolation sample clocks.



**Note** The Total_OSP_Interpolation is the amount of interpolation applied within the *Filtering and Interpolation* component, and does not include the DAC interpolation.

## NI 5442 Prefilter Gain and Offset

You can use the following prefiltering components to add impairments to your data and/or to eliminate overflows that occur later in the <u>OSP</u> block.

#### **Related Topics**

- Prefilter Gain
- Prefilter Offset

## NI 5442 Prefilter Gain

Prefilter gain can change the gain of the I and Q stream during signal generation. You can change the I and Q prefilter gains independently by setting the Pre-Filter Gain I and Pre-Filter Gain Q properties or the NIFGEN_ATTR_OSP_PRE_FILTER_GAIN_I and NIFGEN_ATTR_OSP_PRE_FILTER_GAIN_Q attributes. The gain can range from -2.0 to +2.0 (unitless). Any time the prefilter gain changes, the OSP block ignores all overflows for the next 71 IQ samples. If an overflow occurs during these 71 samples, the data is clipped but an error is not returned. Overflows are common during the first 71 IQ samples after a prefilter gain change because the abrupt change is seen as a transient by the interpolation filters. The prefilter gain can be used to attenuate the IQ data to eliminate overflows in later stages of the OSP block. You can also use the prefilter gain to <u>simulate IQ gain imbalance impairments</u>.

#### **Prefilter Gain Overflow**

Any time the following condition is not true for the I or Q data stream, an overflow occurs when prefilter gain is applied:

 $-1 \leq \text{User Data} \times \text{Prefilter Gain} \leq 1$ 

If an overflow occurs, the data is clipped and NI-FGEN returns an error. To prevent data clipping, attenuate the waveform data or reduce the prefilter gain.



**Tip** To disable error reporting caused by OSP overflows, use the OSP Overflow Error Reporting property or the NIFGEN_ATTR_OSP_OVERFLOW_ERROR_REPORTING attribute.

## NI 5442 Pre-Filter Offset

Prefilter offset can add offset to the I and Q stream during signal generation. You can change the I and Q prefilter offsets independently by setting the Pre-Filter Offset I and Pre-Filter Offset Q properties or the NIFGEN_ATTR_OSP_PRE_FILTER_OFFSET_I and NIFGEN_ATTR_OSP_PRE_FILTER_OFFSET_Q attributes. The offset can range from negative full scale (-1) to positive full scale (+1). Any time the prefilter offset changes, the OSP block ignores all overflows for the next 71 IQ samples. If an overflow occurs during these 71 samples, the data is clipped but an error is not returned. Overflows are common during the first 71 IQ samples after a prefilter offset change because the abrupt change is seen as a transient by the interpolation filters. You can use the prefilter offset to simulate I/Q DC offset impairments.

#### **Prefilter Offset Overflow**

Any time the following condition is not true for the I or Q data stream, an overflow occurs when prefilter offset is applied:

 $-1 \leq$  (User Data × Pre-Filter Gain) + Pre-Filter Offset  $\leq 1$ 

If an overflow occurs, the data is clipped and NI-FGEN returns an error. To prevent data clipping, reduce the <u>prefilter gain</u>, attenuate the waveform data, or reduce the prefilter offset.



**Tip** To disable error reporting caused by OSP overflows, use the OSP Overflow Error Reporting property or the NIFGEN_ATTR_OSP_OVERFLOW_ERROR_REPORTING attribute.

# NI 5442 FIR Filter

NI-FGEN includes a number of built-in lowpass pulse-shaping filters. NI-FGEN calculates the coefficients for each filter. Because the coefficients are scaled for unity-gain, the filters may overflow if transients (such as step response) are presented at the filter input. Use the <u>Filter</u> <u>Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute to set the FIR filter type. The following filters are currently available:

- Flat
- <u>Raised Cosine</u>
- Root Raised Cosine

## NI 5442 FIR Filter Type: Raised Cosine

Alpha Values: 0.1 to 0.4

This lowpass filter is commonly used in communications applications. The passband of the raised cosine filter stops at  $0.5 \times (1 - \alpha)$  of the <u>IQ</u> <u>Rate</u>. The stopband of the raised cosine filter begins at  $0.5 \times (1 + \alpha)$  of the <u>IQ</u> Rate. The transitionband of the raised cosine filter (in dB) follows the following formula:

```
Ideal Raised Cosine Response(f) = 20\log_{10}\left(0.5 + 0.5\cos\left[\frac{\pi(f-S)}{\sigma}\right]\right)
```

where

 $S = 0.5 \times (1 - \alpha)$ 

f = Frequency (fraction of the *IQ Rate*)

Use the Raised Cosine Filter Alpha property or the NIFGEN ATTR OSP FIR FILTER RAISED COSINE ALPHA attribute to set the  $\alpha$  value.

The following diagram shows an ideal raised cosine filter response with an  $\alpha$  of 0.5. The frequency axis is scaled as a fraction of the value of the <u>IQ Rate</u> property or the <u>NIFGEN_ATTR_OSP_IQ_RATE</u> attribute.



## NI 5442 FIR Filter Type: Root Raised Cosine

Alpha Values: 0.1 to 0.4

This lowpass filter is commonly used in communications applications. The passband of the root raised cosine filter stops at  $0.5 \times (1 - \alpha)$  of the *IQ Rate*. The stopband of the root raised cosine filter begins at  $0.5 \times (1 + \alpha)$  of the *IQ Rate*. The transitionband of the root raised cosine filter (in dB) follows the following formula:

Ideal Root Raised Cosine Response(f) =  $20 \log_{10} \sqrt{0.5 + 0.5 \cos \left[\frac{\pi (f-S)}{\alpha}\right]}$ 

where

 $S = 0.5 \times (1 - \alpha)$ 

f = Frequency (fraction of the *IQ Rate*)

Use the Root Raised Cosine Filter Alpha property or the NIFGEN ATTR OSP_FIR_FILTER_ROOT_RAISED_COSINE_ALPHA attribute to set the  $\alpha$  value.

The following diagram shows an ideal root raised cosine filter response with an  $\alpha$  of 0.5. The frequency axis is scaled as a fraction of the value of the <u>IQ Rate</u> property or the <u>NIFGEN_ATTR_OSP_IQ_RATE</u> attribute.


# NI 5442 Filtering and Interpolation

The filtering and interpolation stage of the <u>OSP</u> block increases the effective sample rate of the signal generator while protecting the frequency spectrum of the interpolated data from images. This protection occurs when the data passes through a lowpass filter after zero stuffing. The frequency response of the low pass filter can be changed with the <u>Filter Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute.



## NI 5442 Numerically Controlled Oscillator (NCO)

The numerically controlled oscillator (NCO) is a digital circuit that creates two cosine waves of the same frequency (the <u>carrier frequency</u>) with two independent phases. You can use the <u>Carrier Frequency</u> property or the <u>NIFGEN ATTR OSP CARRIER FREQUENCY</u> attribute to set the carrier frequency. The I phase cosine waveform is multiplied by the I signal path, and the Q phase cosine waveform is multiplied by the Q data path. The I and Q phases are programmable from -180° to 180° by setting the Carrier Phase I and Carrier Phase Q properties or the NIFGEN ATTR OSP CARRIER PHASE I and NIFGEN ATTR OSP CARRIER PHASE Q attributes. The Carrier Phase O property or the NIFGEN ATTR OSP CARRIER PHASE Q only applies when the Data Processing Mode property is set to Complex or the NIFGEN ATTR OSP DATA PROCESSING MODE attribute is set to NIFGEN VAL COMPLEX. Both the frequency and the phases can be updated during generation. For guadrature upconversion, set the I phase to 0° and O phase to -90°. The Carrier Phase I/O properties and attributes can be used to simulate quadrature skew impairments. Change the I or O Carrier Phase by the required guadrature skew to simulate this impairment.

#### NI 5442 IQ Combiner

When the <u>Data Processing Mode</u> property is set to Complex or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute is set to NIFGEN_VAL_COMPLEX, the I and Q data streams are combined after they are multiplied with the carriers. The IQ combiner is implemented as  $I_p - Q_p$ . The combiner block dictates that the following conditions must be true at any given time during the generation, or an overflow can occur:

 $-1 \le I_p Cos(\omega t + \Phi_l) - Q_p Cos(\omega t + \Phi_Q) \le 1$  if the carrier is enabled or

 $-1 \leq (I_p - Q_p) \leq 1$  if the carrier is disabled

where  $I_{\rm p}$  and  $Q_{\rm p}$  are the processed I and Q streams

**Tip** If the OSP block is configured for <u>quadrature upconversion</u>, and the <u>Carrier Phase I</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_PHASE_I</u> attribute is set to 0° and the <u>Carrier Phase Q</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_PHASE_Q</u> attribute is set to -90°, then the IQ combiner must follow the following formula  $(I_p^2 + Q_p^2 \le 1)$  or an overflow can occur.

When an overflow occurs, the data is clipped at the rail where the overflow occurred and the OSP block continues to process data. NI-FGEN returns an error when the status of the signal generator is checked.

P

**Tip** To disable error reporting caused by OSP overflows, use the <u>OSP Overflow Error Reporting</u> property or the <u>NIFGEN_ATTR_OSP_OVERFLOW_ERROR_REPORTING</u> attribute.

# **Basic Onboard Signal Processing Properties**

The following properties must be configured before you can use the OSP block:

- OSP Enabled
- Data Processing Mode
- IQ Rate
- <u>Carrier Enabled</u>
- <u>Carrier Frequency</u>
- FIR Filter Type

## NI 5442 IQ Rate

IQ rate defines the rate at which data is processed by the OSP block. If the <u>Data Processing Mode</u> property is set to Real or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute is set to NIFGEN_VAL_OSP_REAL, then it is the rate at which each sample from waveform memory is taken from memory and inserted into the OSP block. If the Data Processing Mode property is set to Complex or the NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE attribute is set to NIFGEN_VAL_OSP_COMPLEX, then it is the rate at which each complex sample is taken from memory and inserted into the OSP block.

The actual value of the <u>Sample Rate</u> property or the <u>NIFGEN_ATTR_ARB_SAMPLE_RATE</u> attribute is calculated by NI-FGEN based on the IQ rate. NI-FGEN calculates the total OSP interpolation to be used.

Note When onboard signal processing is enabled by setting the <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute, you cannot set the Sample Rate property or the NIFGEN_ATTR_ARB_SAMPLE_RATE attribute .

#### NI 5442 Sample Clock Considerations

The performance of the signal generator that is using the OSP block can be significantly affected by the purity of its Sample clock. Sample clocks with high amounts of jitter or phase noise can create spurs in the signal generator spectrum that are not present when a pure Sample clock is used. If you configure the signal generator for Automatic Clock mode through the <u>Clock Mode</u> property or the <u>NIFGEN ATTR CLOCK MODE</u> attribute, NI-FGEN often selects <u>High-Resolution clocking</u> in order to achieve a specific <u>IQ rate</u>. Because High-Resolution clocking has more jitter than Divide-By-N clocking, extra spurs may occur in the signal generator output spectrum. If you cannot tolerate these spurs, either use a pure external clock as the Sample clock of the signal generator, or use software resampling to change the IQ data to an IQ rate that works with Divide-By-N clocking. If you are resampling, pulse shaping should be done in software and the Filter Type property should be set to Flat or the NIFGEN ATTR OSP FIR FILTER TYPE attribute should be set to NIFGEN VAL OSP FLAT.

# NI 5442 Using an External Clock with the OSP Block

Some applications may require lower jitter or phase noise than the onboard High-Resolution clock. You can use an external clock source to achieve spectral purity at any arbitrary IQ rate. To determine the frequency of the sample rate for the external clock source, complete the following steps.

- 1. Set the <u>Sample Clock Source</u> property or the <u>NIFGEN_ATTR_UPDATE_CLOCK_SOURCE</u> attribute to the external <u>clock source</u> you are using.
- 2. Set the <u>IQ Rate</u> property or the <u>NIFGEN_ATTR_OSP_IQ_RATE</u> attribute.
- 3. Read the value of the <u>Sample Rate</u> property or the <u>NIFGEN_ATTR_ARB_SAMPLE_RATE</u> attribute.
- 4. Set the external clock source sample rate to the frequency of the Sample Rate property or the NIFGEN_ATTR_ARB_SAMPLE_RATE attribute that you just read.
- 5. Validate that the external Sample clock source is connected to the NI 5442 connector specified in the <u>Sample Clock Source</u> property or the <u>NIFGEN_ATTR_SAMPLE_CLOCK_SOURCE</u> attribute and is generating a clock before you continue configuring the NI 5442.

For more information about using external clocks with the NI 5442, refer to <u>External Sample Clock Sources</u>.

#### NI 5442 Carrier Frequency

The carrier frequency determines the frequency of the cosine waves (both I and Q) exported from the <u>NCO</u>. You can use the <u>Carrier</u> <u>Frequency</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_FREQUENCY</u> attribute to set the carrier frequency. This frequency is programmable during signal generation.

For <u>IQ Rates</u> below the interpolation range of the OSP block, NI-FGEN selects a lower Sample clock rate to achieve the requested IQ rate. Because the carrier cannot be more than 0.43 × *Sample Rate*, these lower sample rates translate to lower valid carrier rates.

# NI 5442 FIR Filter Type

The FIR filter type determines the spectral shaping of the data performed in the <u>FIR filter</u>. Use the <u>FIR Filter Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute to set the FIR filter type. The following filter types are supported:

- Flat
- <u>Raised Cosine</u>
- Root Raised Cosine

# **Common Onboard Signal Processing Applications**

The OSP block is particularly useful for the following common applications:

- <u>Arbitrary Waveform Generation</u>
- Single-Tone Generation
- Quadrature Upconversion
- Amplitude Modulation (AM) or Double Sideband
- Baseband Interpolation

# NI 5442 Arbitrary Waveform Generation

The following figure shows the behavior of the OSP block during arbitrary waveform generation.



For normal arbitrary waveform generation, disable onboard signal processing by setting the <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute.

#### NI 5442 Single-Tone Generation

The following figure shows the behavior of the OSP block during singletone generation.



Use the <u>Function Generation mode</u> to generate a single-tone. During single-tone generation, the <u>NCO</u> creates the output signal.

#### NI 5442 Quadrature Upconversion

The following figure shows the behavior of the OSP block during quadrature upconversion.



In quadrature upconversion, you give the I and Q complex waveform data to the OSP block. This data is then pulse–shaped, interpolated up to a high sample rate, and then upconverted to a programmable carrier frequency. For quadrature upconversion, complete the following steps:

- 1. Enable onboard signal processing by setting the <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute.
- 2. Specify the use of complex numbers for the waveform data by setting the <u>Data Processing Mode</u> property or the <u>NIFGEN ATTR OSP DATA PROCESSING MODE</u> attribute.
- 3. Set the <u>IQ Rate</u> property or the <u>NIFGEN_ATTR_OSP_IQ_RATE</u> attribute.
- 4. Set the <u>FIR Filter Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute.
- 5. Set the corresponding filter parameter.
- 6. Enable the carrier by setting the <u>Carrier Enabled</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_ENABLED</u> attribute.
- 7. Set the <u>Carrier Frequency</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_FREQUENCY</u> attribute.
- 8. Download the complex waveform data to the signal generator.
- Note If the complex waveform data has transients, use the <u>Prefilter gain</u> I and Q to attenuate your data and prevent clipping.

#### With Signal Impairments

Signal impairments can be dynamically added to a quadrature upconverted signal. *IQ Gain Imbalance* impairments can be simulated by changing the I or Q prefilter gain. The following formula converts from *IQ Gain Imbalance* (dB, must be negative) to prefilter gain.



**Note** When simulating an IQ gain imbalance, change only the I or Q prefilter gain.

Prefilter Gain = 10^(IQ Gain Imbalance / 20)

I/Q DC offset impairments can be simulated by changing the I and Q prefilter offset. The following formula converts from I/Q DC offset (%) to I/Q prefilter offset.

```
Prefilter Offset = (DcOffset / 100) × Prefilter gain
```

You can simulate quadrature skew impairments by changing the I or Q carrier phase. Change the I or Q carrier phase by the required quadrature skew to simulate this impairment.

## NI 5442 Amplitude Modulation (AM) or Double Sideband

The following figure shows the behavior of the OSP block during amplitude modulation or double sideband.



You can generate an AM radio signal with the OSP block. To generate an AM signal, complete the following steps:

- 1. Enable onboard signal processing by setting the <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute.
- 2. Specify the use of real numbers for the waveform data by setting the <u>Data Processing Mode</u> property or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute.
- 3. Set the <u>IQ Rate</u> property or the <u>NIFGEN_ATTR_OSP_IQ_RATE</u> attribute to the sample rate of the baseband data.
- 4. Set the <u>Pre-Filter Gain I</u> property or the <u>NIFGEN_ATTR_OSP_PRE_FILTER_GAIN_I</u> attribute to 0.5.
- 5. Set the <u>Pre-Filter Offset I</u> property or the <u>NIFGEN_ATTR_OSP_PRE_FILTER_OFFSET_I</u> attribute to 0.5. Steps 4 and 5 ensure that all interpolated data is positive when it is mixed with the carrier.
- 6. Enable the carrier by setting the <u>Carrier Enabled</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_ENABLED</u> attribute.
- 7. Set the <u>Carrier Frequency</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_FREQUENCY</u> attribute to the station frequency.
- 8. Specify a flat FIR filter by setting the <u>FIR Filter Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute.
- 9. Set the <u>Flat Filter Passband</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_FLAT_PASSBAND</u> attribute to

0.4.

10. Download the waveform data to the signal generator.

## NI 5442 Baseband Interpolation

The following figure shows the behavior of the OSP block during baseband interpolation.



Baseband interpolation allows the OSP block to interpolate signals at a low sample rate up to a high sample rate. Pulse shaping of the data can also be done in the FIR filter. For baseband interpolation, complete the following steps.

- 1. Enable onboard signal processing by setting the <u>OSP Enabled</u> property or the <u>NIFGEN_ATTR_OSP_ENABLED</u> attribute.
- 2. Specify the use of real numbers for the waveform data by setting the <u>Data Processing Mode</u> property or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute.
- 3. Set the <u>IQ Rate</u> property or the <u>NIFGEN_ATTR_OSP_IQ_RATE</u> attribute to the low sample rate of the waveform data.
- 4. Set the <u>FIR Filter Type</u> property or the <u>NIFGEN_ATTR_OSP_FIR_FILTER_TYPE</u> attribute.
- 5. Set the corresponding filter parameter or download a <u>custom set</u> <u>of FIR filter coefficients</u>.
- 6. Disable the carrier by setting the <u>Carrier Enabled</u> property or the <u>NIFGEN_ATTR_OSP_CARRIER_ENABLED</u> attribute.
- 7. Download the low sample rate waveform(s) to the signal generator.

#### NI 5442 Sample Size and Resolution

The NI 5442 stores arbitrary waveforms in memory as signed 16-bit digital words. On the NI 5442, the entire 16 bits are sent to the digital gain circuit, the digital filter and the DAC.

The NI 5442 stores arbitrary *complex* waveforms in memory as interleaved real/imaginary 16-bit digital words. Each real/imaginary pair is processed by the OSP block before it is sent to the digital gain circuit, the digital filter, and the DAC.

#### **Related Topics**

Onboard Memory

Waveform Sizes

#### NI 5442 Minimum Waveform Size and Quantum

#### Waveform Size

The NI 5442 onboard memory architecture imposes certain requirements on the waveform size and quantum. The minimum waveform size depends on the output mode and the <u>trigger mode</u>. Refer to the <u>device</u> <u>specifications</u> for the minimum waveform size values for the different modes.

Note To provide greater programming flexibility, NI-FGEN does not strictly enforce the minimum waveform sizes stated in the <u>device specifications</u>. NI-FGEN enforces a minimum waveform size of four samples for all trigger modes (two if the OSP block is enabled and the waveform data points have been configured for complex data using the <u>Data Processing Mode</u> property or the <u>NIFGEN_ATTR_OSP_DATA_PROCESSING_MODE</u> attribute), so it is possible to generate waveforms that are smaller than the sizes given in the specifications. However, the device may not be able to fetch data from onboard memory fast enough to keep up with waveform generation at high sample rates.

This condition may occur if a segment is looping over a very small waveform, if a segment is generating a marker within a very small waveform, or if triggers are advancing the segments in a sequence very rapidly. When this occurs, NI-FGEN reports Error – 1074115901 (0xBFFA4AC3): Device Data Underflow.

The simplest way to avoid this condition is to follow the minimum waveform size guidelines in the specifications. If these rules are followed, a data underflow error will not occur under any sample rate. You can develop applications that generate waveforms smaller than those listed in the device specifications at slower sample rates. If a data underflow occurs, NI-FGEN reports the error when the generation is aborted. This is typically accomplished by calling the niFgen Abort Generation VI or the niFgen AbortGeneration function, or if you call the niFgen Wait Until Done, or niFgen Is Done VIs (or the niFgen_WaitUntilDone or niFgen_IsDone functions) while the device is generating a signal. To monitor error conditions during waveform generation, the niFgen Is

Done VI or the niFgen_IsDone function can be called repeatedly while the device is generating a signal.

#### Quantum

Quantum is the increment in samples for waveform sizes. The NI 5442 has a sample quantum of one, allowing waveforms of any size (between the maximum and minimum waveform sizes) to be downloaded.

The maximum waveform size allowed depends on the remaining available space in the onboard memory of the device. The remaining available space depends on factors such as any waveforms and generation instructions currently occupying memory space in the onboard memory. The maximum allowable size equals the <u>memory size</u> of the device minus the data already in memory. Query the <u>Max Waveform Size</u> property or the <u>NIFGEN_ATTR_MAX_WAVEFORM_SIZE</u> attribute for the current largest size waveform that can be downloaded to the device.

You can download floating point, signed 16-bit binary, or complex floating-point waveforms to the device onboard memory. For information about downloading waveforms to the onboard memory in LabVIEW, refer to the <u>niFgen Create Waveform</u> or <u>niFgen Write Waveform</u> VIs for more information. For information about downloading waveforms to the onboard memory in C, refer to the <u>niFgen_CreateWaveformF64</u>, <u>niFgen_CreateWaveformI16</u>, <u>niFgen_CreateWaveformComplexF64</u>, <u>niFgen_WriteWaveform, niFgen_WriteBinary16Waveform</u>, or <u>niFgen_WriteWaveformComplexF64</u> functions for more information.

#### NI 5442 Marker Events

A marker is an event that the device generates in relation to a waveform that is generated. The event is configured to occur at the time that a specific location or sample *n* in the waveform generates on the CH 0 connector. If the waveform loops multiple times in a segment, the marker generates each time the waveform loops. The following figure shows a pulse that represents a waveform sample *n* that is one Sample clock in width of a waveform being generated on the CH 0 connector. The second pulse, the Marker event, represents the pulse that generates when the corresponding waveform sample *n* generates at the CH 0 connector. Refer to Features Supported to determine if your device supports markers.



 $t_{m1}$  represents the delay in time of the Marker event generated relative to the configured waveform sample *n* being generated.

t_{m2} represents the Marker event pulse width in time.

NI-FGEN takes into account the factors that affect the delays in the Digital and Analog paths in assuring that the Marker event appears within one Sample clock of the waveform output. Therefore,  $t_{m1}$  is less than one Sample clock period.

The Marker event pulse width,  $t_{m2}$ , is at least 150 ns and can be significantly longer than 150 ns for slower Sample clocks. You can configure the pulse width by setting the <u>Marker Event Pulse Width</u> property or the <u>NIFGEN_ATTR_MARKER_EVENT_PULSE_WIDTH</u> attribute. Instruments commonly have a minimum pulse width specification for a trigger to be registered, and trigger pulses of smaller widths are ignored. The signal generator ensures that a minimum pulse width exists on the Marker event by using a pulse stretching circuit. A Sample clock rate of 100 MS/s has a period of 10 ns, requiring the pulse to be lengthened for many devices to register the marker as a good trigger pulse. Refer to the <u>device specifications</u> for the timing specifications.

#### **Creating Markers**

You can specify a marker and its location by setting an offset location value (in number of samples) from the start of the waveform. If the offset is out of range of the number of samples in that segment, NI-FGEN returns an error.



**Note** In Burst trigger mode, a marker must be placed at least twenty four samples from the end of the waveform.

To create a marker in <u>Arbitrary Waveform Mode</u>, set the <u>Arbitrary</u> <u>Waveform Marker Position</u> property or the <u>NIFGEN_ATTR_ARB_MARKER_POSITION</u> attribute. Then use the <u>niFgen Export Signal</u> VI or the <u>niFgen_ExportSignal</u> function to export the marker signal.

To create a marker in <u>Arbitrary Sequence Mode</u>, refer to the **Marker Location Array** parameter of the <u>niFgen Create Advanced Arb</u> <u>Sequence</u> VI or the **markerLocationArray** parameter of the <u>niFgen_CreateAdvancedArbSequence</u> function. Then use the niFgen Export Signal VI or the niFgen_ExportSignal function to export the marker signal.

In <u>Script mode</u>, you can create up to four markers for each waveform. To create markers in Script mode, refer to the *NI Script Editor Help*. Then use the niFgen Export Signal VI or the niFgen_ExportSignal function to export the marker signal.



**Note** When exporting markers in Script mode, you must specify the marker using the **Signal Identifier** parameter of the niFgen Export Signal VI or the **signalIdentifier** parameter of theniFgen_ExportSignal function.

#### Markers as Trigger Outputs

A delay of at least 44 Sample clocks exists between the Start trigger and the analog waveform generation on the output connector. Therefore, synchronizing the signal generator output signal to other devices with fast trigger response times is accomplished using the Marker event from the signal generator as the trigger source for the other device for more precise alignment to the generating waveform. You can do this using the RTSI bus, PXI trigger lines, SYNC OUT/PFI 0 and PFI 1 or PFI 4 and PFI 5. Refer to Exporting Signals for more information about routing signals off the device.

Note Devices without a DDC connector do not support PFI <4..5>.

## NI 5442 Exporting Signals

The signal generator contains seven PXI trigger lines that are available for sending signal generator-specific information to other devices that have PXI trigger or RTSI bus connectors.

The signal generator has connectors on the front panel to route signals to devices external to the PXI Express chassis. The following table shows the signals available for export and the lines they can be routed to. To determine all possible signal routes for your device, refer to <u>Signal</u> <u>Routing</u>.

		Destination	
		PXI_TRIG<06>	PFI 0 and PFI 1 Connectors
Exported Clocks, Triggers, and Events	Sample Clock	Yes	Yes*
	Sample Clock Timebase	Yes	Yes
	PLL Reference Source	Yes	Yes*
	Out Start trigger	Yes	Yes
	Marker Event	Yes	Yes
*Note PFI 0 is optimized for the Sample clock and PLL Reference clock			

*Note PFI 0 is optimized for the Sample clock and PLL Reference clock source signals and has slightly less jitter than PFI 1. PFI 0 is the recommended terminal to use for exporting clocks.

**Sample Clock**—The clock signal that tells the DAC when to convert the digital waveform values to an analog voltage. The Sample clock frequency is referred to as the Sample clock rate; the rate at which the digital waveforms from device memory are generated. The Sample clock is also known as update clock.



Notes The Sample clock can be exported directly, or it can first be

divided down by an integer. This configuration provides a variable frequency signal related to the waveform sample rate to synchronize other devices to the generation.

NI does not recommend exporting clocks greater than 20 MHz over PXI_TRIG<0..6>.

If you export the divided-down Sample clock to another device to synchronize sampling, you can also use the Sample clock as the Start trigger for the signal generator. Using the divided-down Sample clock as the Start trigger begins signal generation at the same place each time relative to the divided-down Sample clock. This technique is more useful as the divisor becomes larger and, while an improvement over using an immediate Start trigger, there remains an uncertainty of one Sample clock.

**Sample Clock Timebase**–The 100 MHz clock signal from which the internal Sample clock is derived. The Sample clock timebase is also know as board clock.



**Note** The Sample clock timebase (board clock) is always exported after being divided-down. The default divide-down value is 2. Valid divide-down values range from 2 to 4,194,304.

If you export the Sample clock timebase to another device to synchronize sampling, you can also use the Sample clock timebase as the Start trigger for the signal generator. Using the Sample clock timebase as the Start trigger begins signal generation at the same place each time relative to the Sample clock timebase. This technique is more useful as the divisor becomes larger and while an improvement over using an immediate Start trigger there remains an uncertainty of one Sample clock.

**PLL Reference clock source**–A clock signal that is only available when a PLL Reference source has been configured. The clock is the source selected as the PLL Reference clock source.

**Out Start trigger**–A signal generated by the device upon recognizing a start condition that can be routed out various connectors to signal other devices.

Marker event-A digital signal that can be used as a trigger

corresponding to a specific sample in the waveform generation. This signal controls other devices that require timing information related to a specific point in the generated waveform.

#### **Routing Signals**

You can route signals in the following ways:

- The Marker event generated during an Arbitrary Waveform Generation mode waveform generation to any of the PXI trigger lines or front panel connectors.
- The signal generator Start trigger output signal to other devices through any of the PXI trigger lines or front panel connectors.
- The signal generator Sample clock signal to other devices through any of the PXI trigger lines or front panel connectors.
- The PLL Reference clock source to other devices through any of the PXI trigger lines or front panel connectors.

In NI-FGEN, the PXI trigger lines are referred to as RTSI<0..6>. The correlation between PXI_TRIG<*x*> and RTSI<*x*> is one to one. For more information about configuring and routing the device internal signals, refer to the niFgen Export Signal VI or the niFgen_ExportSignal function.

# **Integration and System Considerations**

This section contains information about integrating NI signal generators into a PXI-based or a PCI-based measurement system.

The PXI architecture has built-in timing and triggering features that can synchronize multiple devices over a backplane timing bus. Multiple devices in a modular instrumentation system can share a common Reference clock and synchronize to triggers that are distributed over controlled signal paths that ensure matched propagation. PC plug-ins with RTSI also provide an internal bus that can be accessed by multiple devices. Internal routing of these timing signals in PXI and PC plug-ins with RTSI eliminate complicated external wiring. Standardized timing protocols eliminate incompatibilities, giving you the best performance when synchronizing any kind of analog, digital, or timing measurements.

#### Integration and System Considerations Environment

Device performance and reliability may be limited at temperatures above the specified operating range. For best performance take the following precautions:

- Ensure that the ambient temperature is within the specifications for the device and is stable (±5 °C).
- Follow standard metrology practices.
- Use a PXI or PXI Express chassis with a well-designed cooling system.

Operating NI PXI and PXI Express signal generators outside the specified operating temperatures can increase bias currents in the electronic components, increase noise, accelerate drifts, and decrease product life. Beyond the maximum specified operating temperatures, the device may perform differently than during factory calibration, resulting in additional measurement errors. Also, operating the device outside of the humidity specification (>80%, >35 °C) may cause leakages between circuit components and introduce measurement error.

To optimize cooling and ensure best performance and reliability the use the following guidelines:

• Chassis that provide multiple fan speed settings should always be run with fans set on high or auto if applicable to your chassis. Never set the fans to low or turn them off.



**Note** In newer NI chassis the settings are HIGH and AUTO, in some older NI chassis the fan settings may be HI and LO.

- All empty slots in the chassis should be covered with a blank slot filler panel.
- Remove and clean the inlet filters often to prevent buildup of dust and other foreign material that may restrict airflow.
- The chassis should be located such that the fan inlets and outlet vents are not obstructed. Other objects and equipment should be kept a minimum of 3 inches from the fan inlets.

For more information about forced-air cooling, refer to your chassis

documentation.

NI PXI and PXI Express signal generators are designed to operate at shock up to 30 g, 11 ms, half-sine. It is specified to withstand shock up to 50 g, 11 ms, half-sine when not operating (shipping/storage).

NI PXI and PXI Express signal generators are designed to withstand total random vibration of 0.31  $g_{rms}$  operational and 2.46  $g_{rms}$  non operational per IEC 68-2-64.

#### Integration and System Considerations PXI/PXI Express Chassis Cooling

Not all PXI or PXI Express chassis provide the same cooling. When selecting a PXI or PXI Express chassis, consideration should be given to providing adequate airflow for high power and sensitive devices such as NI signal generators.

NI PXI and PXI Express signal generators are high-precision instruments and may be sensitive to interference from other electronic devices. To optimize the accuracy and performance of the device, you may need to locate the device in a slot away from devices with power supplies and other noisy circuitry. The device may also be sensitive to heat generated by high-power products in neighboring slots. When possible, consider locating the device away from high-power devices to optimize cooling.

# Integration and System Considerations PXI Modules

PCI eXtensions for Instrumentation (PXI) modular instrumentation delivers a PC-based, standardized, high-performance measurement and automation system. PXI combines the high-speed PCI bus with integrated timing and triggering designed specifically for measurement and automation applications to deliver significant performance improvements over older architectures. The following figure shows a typical PXI chassis installation.


### NI Signal Generators Available as PXI Modules

The NI 5401/5402/5404/5406/5411/5412/5421/5422/5431/5441 signal generators are available in the PXI form factor.

### **Chassis Guidelines**

NI PXI signal generators can be installed in the following chassis and slots:

- **PXI chassis**—PXI signal generators can be installed in any peripheral slot of a PXI chassis.
- **PXI-Express chassis**—PXI signal generators can be installed in the following PXI Express chassis slots:
  - PXI-1 slots—Accepts PXI modules
  - PXI hybrid slots—Accepts either PXI modules that are hybrid slot-compatible or PXI Express modules

### Using PXI-Compatible Products with Standard CompactPCI Products

The ability to use PXI-compatible products with standard CompactPCI products is an important feature provided by the *PXI Specification*, revision 2.1. If you use a PXI-compatible plug-in device in a standard CompactPCI chassis, you cannot use PXI-specific functions, but you can still use the basic plug-in device functions. For example, the PXI trigger bus on NI signal generators is available in a PXI chassis but not in a CompactPCI chassis. The CompactPCI specification permits vendors to develop sub-buses that co-exist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. NI signal generators work in any standard CompactPCI chassis. PXI-specific features, such as PXI_Trig bus and PXI_CLK10 reference are implemented on the J2 connector of the CompactPCI bus.

### **Related Topics**

### PXI Star Trigger Line

### **Related Web Topics**

For an overview of the PXI Specification, refer to <u>PXI Specification</u> <u>Tutorial</u>

For an overview of PXI-specific functions, refer to <u>How do National</u> <u>Instruments PXI Boards map to the PXI Backplane?</u>

### Integration and System Considerations PXI Express Modules

The PXI Express Specification integrates PCI Express signaling into the PXI standard, which increases backplane bandwidth and enhancing PXI timing and synchronization features while maintaining backward compatibility with PXI.



### NI Signal Generators Available as PXI Express Modules

The NI 5442 arbitrary waveform generator is available in the PXI Express form factor.

### **Chassis Guidelines**

NI PXI Express signal generators can be installed in the following PXI Express chassis slots:

- **PXI hybrid slots**—Accepts either PXI modules that are hybrid slotcompatible or PXI Express modules
- PXI Express slots—Accepts PXI Express modules



**Note** Refer to the documentation for your PXI Express device and chassis for more information about installing and configuring PXI Express modules.

## Using PXI Express Products with CompactPCI Express Products

The CompactPCI/PXI Express backplane integrates PCI Express while still preserving compatibility with current PXI modules. PXI Express hybrid slots are capable of delivering signals for both PCI and PCI Express. Thus, the hybrid slot allows you to install a PXI module that uses PCI signaling or a PXI Express module that uses PCI Express signaling.

### **Related Web Topics**

For an overview of the PXI Express specification, refer to <u>PXI Express</u> <u>Specification Tutorial</u>

## Integration and System Considerations PXI Star Trigger Line

The PXI Star trigger is a feature implemented on National Instruments PXI chassis. PXI chassis have a PXI trigger bus that is linked to all slots in the chassis. In addition, PXI chassis have a PXI Star trigger that is linked to the system timing slot (Slot 2 on PXI chassis). The PXI Star trigger is a high-performance trigger signal that you can use to synchronize all the devices in a chassis. You can also do this using the normal PXI trigger bus, but the PXI Star trigger offers increased performance, specifically a propagation delay of no more than 5 ns and skew of no more than 1 ns.



The PXI Star trigger lines allow a PXI Star controller in Slot 2 to route signals to or from other peripheral slots with very low skew and at higher bandwidth than other PXI trigger lines.

When not using PXI Star, you can use Slot 2 as a standard peripheral slot. However, when using PXI Star, you must have a PXI Star controller, (master) device in Slot 2, and one or more peripheral devices in the other slots.

If placed in a peripheral slot—Slot 3 or higher—all NI PXI signal generators can receive a signal from PXI Star.

Additionally, an NI 5402/5406/5412/5421/5422/5441 in a peripheral slot can be configured to route a signal onto the PXI Star line if the PXI Star trigger controller is configured to receive it.



**Note** PXI Express signal generators in PXI Express chassis can

import clocks on the PXI Star line. However, PXI Express signal generators cannot import triggers or export clocks or triggers over the PXI Star line.

**Related Topics** 

PXI Modules

# Integration and System Considerations PXI Trigger Lines

Eight PXI bus trigger lines are highly flexible and can be used in a variety of ways. For example, triggers can be used to synchronize the operation of several different PXI peripheral devices. In other applications, one device can control carefully timed sequences of operations performed on other devices in the system. Triggers may be passed from one device to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. The number of triggers that a particular application requires varies with the complexity and number of events involved.



The PXI Specification is implemented with the RTSI bus through the PXI trigger lines. PXI Specification requires eight lines, PXI_Trig<0..7>, on the P2/J2 connector of the PXI chassis for the trigger lines. The RTSI features of NI signal generators is implemented on this sub-bus. The RTSI triggers <0..6> are implemented on PXI_Trig<0..6>, and the RTSI clock is routed on PXI_Trig7.

For an overview of PXI-specific functions, refer to <u>How do National</u> <u>Instruments PXI Boards map to the PXI Backplane?</u>

### **Related Topics**

PXI Star Trigger

### Integration and System Considerations System Reference Clock, PXI_CLK10

The PXI chassis supplies the PXI 10 MHz system Reference clock signal (PXI_CLK10) independently to each peripheral slot. An independent buffer drives the clock signal to each peripheral slot. The buffer has a source impedance matched to the backplane and a skew ranging from less than 1 ns to better than 250 ps between slots. You can use this common Reference clock signal to synchronize multiple devices in a measurement or control system. You can drive PXI_CLK10 from an external source through the PXI_CLK10_IN pin on the P2 connector of the PXI Star trigger slot, which is slot 2. Sourcing an external clock on this pin automatically disables the 10 MHz source on the backplane. You can synchronize multiple chassis that have connectors on the back panel for 10 MHz reference in and 10 MHz reference out. Refer to your PXI chassis documentation for more information.

## Integration and System Considerations PFI Lines

PFI lines are multipurpose programmable function input/outputs. These lines serve as connections to virtually all internal timing signals. NI signal generators have up to six digital lines that can accept or generate a trigger, generate a marker, accept or generate a Reference clock. The function of each PFI line is independent.

If you are using LabVIEW to program your signal generator and you want to connect external signal generators to the PFI lines, you can use the <u>niFgen Configure Sample Clock Source</u> VI, the <u>niFgen Configure</u> <u>Reference Clock</u> VI, or the <u>niFgen Configure Trigger</u> VI to route external signals to internal sources. You can use the <u>niFgen Export Signal</u> VI to route internal signals to the PFI lines on the front panel.

If you are using LabWindows/CVI to program your signal generator, you can use the <u>niFgen_ConfigureSampleClockSource</u> function, the <u>niFgen_ConfigureReferenceClock</u> function, or the <u>niFgen_ConfigureTriggerSource</u> function to route external signals to internal sources. You can use the <u>niFgen_ExportSignal</u> function to route internal signals to the PFI lines on the front panel.

**Caution** If you enable a PFI line for output, do *not* connect any external signal source to it; doing so can damage the device, the computer, and the connected equipment.

### **Related Topics**

NI PXI-5404 PFI 0 Connector NI PXI/PCI-5421/5422/5441 CH 0 Connector

## **MXI-3 Optimization Application**

If you are using the MXI-3 interface to control the PXI chassis, the MXI-3 Optimization Application must be run prior to using the NI signal generator. By default, this application runs automatically when Windows starts. If you have an initialization, timeout, or performance issue with your module, or if you are not certain that the application ran, select **Start»All Programs»National Instruments MXI-3»MXI-3 Optimization** to run the application. If you continue to have initialization or performance issues, refer to the MXI-3 documentation at **Start»All Programs»National Instruments MXI-3**, or visit NI Technical Support at ni.com/support.

## **MXI-4 and MXI-Express Optimization**

Optimization for MXI-4 and MXI Express are performed automatically by the hardware.

### Integration and System Considerations PCI Chassis Cooling

Not all PCI chassis provide the same cooling, when selecting a PCI chassis, consideration should be given to providing adequate airflow for high power and sensitive devices such as NI PCI signal generators.

NI PCI signal generators are high-precision instruments and may be sensitive to interference from other electronic devices. To optimize the accuracy and performance of the device, you may need to locate the device in a slot away from devices with power supplies and other noisy circuitry. The device may also be sensitive to heat generated by highpower products in neighboring slots. When possible, consider locating the device away from high-power devices to optimize cooling.

### Integration and System Considerations RTSI Bus

RTSI stands for Real-Time System Integration. It is a bus found on many National Instruments devices that, when cabled together with a RTSI cable, is used to share and exchange timing and control signals between multiple boards. It is usually used for synchronization purposes.



The previous figure shows an example of an extended five-board cable setup.

The RTSI bus cables are short, 34-conductor ribbon cables equipped with two to five connectors to link together a group of boards. The cable options include connections for two, three, four, and five boards, plus an extended cable length to connect up to five long and short boards.

# Integration and System Considerations Synchronization

Synchronization occurs when two or more measurement devices operate in step with a common Reference clock. You can synchronize NI signal generators with other instruments, including digitizers and digital I/O devices, or you can synchronize several signal generators with each other.

For an overview of synchronization, refer to <u>Think Synchronization First</u> to <u>Optimize Automated Test</u> at NI Developer Zone.

For information about synchronizing multiple NI 5421/5422/5441 signal generators, refer to <u>Multiple Module Synchronization</u>.

## **Interactive Tools**

Expand this topic for information about any installed software tools you can use with your NI signal generator.

## **FGEN Soft Front Panel**

The FGEN Soft Front Panel (SFP) can be used to interactively generate waveforms with your NI signal generators module. For information about developing applications to generate waveforms, refer to <u>Programming</u>.

Similar to stand-alone instruments, the FGEN SFP controls and presents data. However, because it operates on the PC, it provides additional processing, storage, and display capabilities.

You can access the FGEN SFP at **Start»All Programs»National Instruments»NI-FGEN»FGEN Soft Front Panel**. In addition to this help file, you can learn more about using the FGEN SFP by launching the FGEN SFP, and selecting **Help»Show Context Help** or by pressing <Ctrl+H>.

## FGEN SFP: Function Library

**Function**—A function, with respect to the FGEN SFP, is one period of a continuous signal that can be generated with a DDS clocking scheme.

The FGEN SFP provides internal libraries to create common mathematical functions for <u>DDS mode</u> only.

### **Available Functions**

Haversine

Havertriangular

Trapezoid	(Delay Time in %, Rise Time in %, Hold Time in %, Fall Time in %)
Sinc	(Number of periods in addition to main loop)
Exponential Rise	(Time constant t relative to function length)
Exponential Fall	(Time constant t relative to function length)
Triangular Nois	Se
Gaussian Whit	e Noise

### FGEN SFP: Waveform File Specifications

- Binary Waveform Data Format (.bin)
- Frequency Shift-Keying Source File
- LabVIEW Measurement Data File (.lvm)

## FGEN SFP: Binary Waveform Data Format (.bin)

The FGEN SFP can import data from a binary file that conforms to the following specifications:

- File extension—.bin
- File header-none
- Data—Data are stored as a continuous single stream. You must remember the data type you stored the data in. Data can be imported in 8-, 16-, or 32-bit binary, and can be little or big endian format.

## FGEN SFP: Frequency Shift-Keying Source File Specifications

The frequency shift-keying file is used to describe time relations of frequency hopping between frequency 0 and frequency 1. It corresponds with applications in the communication industry where data can be stored in binary or hexadecimal values.

A frequency shift-keying file must start with a character identifier for data parsing. The identifier for binary values is 'binary' and 'hexadecimal' for hexadecimal values. After the identifier, the file can contain an unlimited amount of header information. A carriage return (non-printable character \r\n) marks the start of the data. After the carriage return, the data must follow a continuous stream without any delimiters. The end of data is defined as the first character not valid for specified identifier; a non-printable delimiter or the end of a file.

### Example

## FGEN SFP: LabVIEW Measurement Data File (.lvm)

The LabVIEW Measurement (.lvm) format is a text-based file format for one-dimensional data that you can use with the Read LabVIEW Measurement File and Write LabVIEW Measurement File Express VIs.

The .lvm format is easy to parse and easy to read when imported into a spreadsheet program such as Microsoft Excel, or a text editor such as Notepad. The .lvm format supports multiple data sets, grouping of data sets, and the addition of data sets to existing files.

The file format is not designed for high performance or for very large data sets, as is the case with all text-based formats.



**Note** For very large data sets, use the binary file format.

For more information about the .lvm file format, refer to the specification at <u>NI Developer Zone</u>.

## FGEN SFP: Example Files

The following table contains descriptions of the example files. For the installation locations of these files, refer to the <u>NI-FGEN Instrument</u> <u>Driver Readme</u>.



**Note** For more information about the .lvm file format, refer to the *LabVIEW Express Measurement File Specification v. 0.92* at <u>NI</u> <u>Developer Zone</u>.

File Name	Description
fgMode-square.bin	A <u>binary</u> file that contains 16,384 16-bit samples in little endian format. The waveform pattern represented in the file is a single period of a square pattern with a high duty cycle of 20%.
arbMode- Testsignal.bin	A binary file that contains 50,000 16-bit samples in little endian format. The waveform pattern contains five periods of a sine waveform pattern, 5 periods of a square waveform pattern, 5 periods of a triangular waveform pattern, 4.5 periods of a sawtooth waveform pattern, and a stairstep pattern with 10 steps. The length of each step in the stairstep waveform pattern is equal to the length of ¹ / ₂ period of the previous pattern.
arbMode-sine.lvm	A text-based file containing six waveforms of 400 samples each. The file conforms to the <i>LabVIEW</i> <i>Express Measurement File Specification v.0.92</i> . Each set of waveform data in this file represents multiple periods of a sine waveform pattern. Each line after the header (starting with line 24) is organized into columns separated by a <tab> character. The first column is empty, normally holding the relative time in seconds from the first sample. The second through seventh columns</tab>

	contain data values whose maximum amplitude is ±1 V. The last column contains comments.
arbMode-square.lvm	A text-based file containing four waveforms of 400 samples each. The file conforms to the <i>LabVIEW</i> <i>Express Measurement File Specification v. 0.92</i> . Each set of waveform data in this file represents multiple periods of a square waveform pattern. Each line after the header (starting with line 24) is organized into columns separated by a <tab> character. The first column is empty, normally holding the relative time in seconds from the first sample. The second through fifth columns contain data values whose maximum amplitude is ±1 V. The last column contains comments.</tab>
arbMode- triangular.lvm	A text-based file containing four waveforms of 400 samples each. The file conforms to the <i>LabVIEW</i> <i>Express Measurement File Specification v. 0.92</i> . Each set of waveform data in this file represents multiple periods of a triangular waveform pattern. Each line after the header (starting with line 24) is organized into columns separated by a <tab> character. The first column is empty, normally holding the relative time in seconds from the first sample. The second through fifth columns contain data values whose maximum amplitude is ±1 V. The last column contains comments.</tab>
arbMode-rampup.lvm	A text-based file containing four waveforms of 400 samples each. The file conforms to the <i>LabVIEW</i> <i>Express Measurement File Specification v. 0.92</i> . Each set of waveform data in this file represents multiple periods of a ramp up waveform pattern. Each line after the header (starting with line 24) is organized into columns separated by a <tab> character. The first column is empty, normally holding the relative time in seconds from the first sample. The second through fifth columns contain data values whose maximum amplitude is ±1 V. The last column contains comments.</tab>

arbMode- rampdown.lvm	A text-based file containing four waveforms of 400 samples each. The file conforms to the <i>LabVIEW</i> <i>Express Measurement File Specification v. 0.92</i> . Each set of waveform data in this file represents multiple periods of a ramp down waveform pattern Each line after the header (starting with line 24) is organized into columns separated by a <tab> character. The first column is empty, normally holding the relative time in seconds from the first sample. The second through fifth columns contain data values whose maximum amplitude is ±1 V. The last column contains comments.</tab>
arbMode-noise.lvm	A text-based file containing 512 samples. The file conforms to the <i>LabVIEW Express Measurement</i> <i>File Specification v. 0.92</i> . The data in this file represent uniform white noise. Each line after the header (starting with line 24) is organized into columns separated by a <tab> character. The first column is empty, normally holding the relative time in seconds from the first sample. The second column contains a data value whose maximum amplitude is ±1 V. The last column contains comments.</tab>
FList_ExampleFile.txt	Contains a frequency list designed for NI signal generators. The first column in this sequence represents a frequency to be generated for the amount of time specified in column two (duration). This frequency list contains 516 entries. The last four entries and the 512 th entry are different from the rest of the list to distinguish the last entry output when imported into an NI PXI/PCI- 5401/5411/NI-5431 signal generator.
FSK_ExampleFile.txt	An example showing how <u>FSK</u> data must be set u to import it into the FGEN Soft Front Panel. This file contains 138 binary data bits.

## **Using the NI Video Generator Wizard**

Select Start»Programs»National Instruments Composite Video Generator»Video Generator Wizard to launch the NI Video Generator Wizard. The dialog box shown in the following figure appears.

Nideo Generator Wizard	
<ul> <li>Load video data file from disk</li> <li>Load BMP file and compute video data</li> <li>BMP Input File Path</li> <li>C:\Program Files\National Instruments\Ni-vi</li> </ul>	Browse Display BMP Device ID
<ul> <li>Use factory settings</li> <li>Use custom settings</li> <li>Edit factory settings</li> <li>Edit custom settings</li> </ul>	<ul> <li>M-NTSC</li> <li>Standard PAL</li> <li>M-PAL</li> <li>N-PAL</li> <li>Combination N-PAL</li> <li>SECAM</li> </ul>
<ul> <li>Download video data file</li> <li>Save video data file to disk</li> <li>Save and Download</li> </ul>	Exit Finish

The NI Video Generator Wizard uses or generates three file types as follows:

- .bmp—The bitmap image representing the basic RGB image to be reproduced by the video generator.
- .cfg—The configuration file where you can save the specific video settings. The video settings include the video parameters or attributes, which are the signal conditions, the video format such as PAL or NTSC, and some other information. You can edit these video settings by choosing Edit factory settings or Edit custom settings the NI Video Generator Wizard dialog box.
- .bin—16-bit file format used to save the data of a complete

composite video signal. With this file format, you can save or recall binary video data files to or from disk.

When you select the different options in the NI Video Generator Wizard dialog box, you use or generate the three different files types described above.

## Loading BMP File and Computing Video Data

If you select **Load BMP file and compute video data** in the upper section of the dialog box and select **Use factory settings**, you can then select the video format you want to generate, such as **M-NTSC**, and create a video signal based on a specified bitmap image file. The factory (default) settings generate a video signal that respects the video norm of the selected video format.

By selecting the **Edit factory settings** option in the middle section of the Video Generator Wizard dialog box, you can edit the factory settings for the generated video signal. You can also recall, using Use custom settings, or recall and edit, using Edit custom settings, a previously saved configuration file. Refer to <u>Editing Video Parameters</u> for more information.

In the bottom section of the dialog box, you can download a binary video data file and start generating the video signal, using Download video data file, and/or save the binary video data file to disk, using Save video data file to disk. For more information, refer to <u>Downloading and Saving a</u> <u>Video Data File</u>.

## **Generating a Video Signal**

To generate a video signal based on a bitmap image using the factory settings, select the proper options in the NI Video Generator Wizard dialog box.

In generate a video signal, complete the following steps:

- 1. Make sure that the device ID is set to the correct value (configured by MAX).
- 2. Select Load BMP file and compute video data.
- 3. Click Browse.
- 4. Double-click the appropriate directory from the following:
  - For NTSC users, double-click the 640x480 or the 1044x480 directory.
  - For PAL and SECAM users, double-click the 768x576 or the 1040x576 directory.
- 5. Double-click any of the example .bmp files. The bitmap image file path now appears in BMP Input File Path.
- 6. On the left side of the dialog box, select **Use factory settings**. This option applies the default video parameters to the video signal you are going to generate.
- 7. On the right side of the dialog box, select **M-NTSC**, **Standard-PAL**, or **SECAM**, depending on the video format you want to generate.
- 8. Select **Download video data file**. This option downloads the binary video data from the computer to the NI PXI/PCI-5431.
- 9. Click **Finish**. A Processing dialog box appears to show you the processing status.
- Note If you select **Display BMP** next to Browse, when you click **Finish** in step 9, you can see the .bmp file displayed on the computer monitor.

Based on the .bmp file you selected, the NI Video Generator Wizard calculates an NTSC, PAL, or SECAM video data, downloads the calculated data to the NI 5431, and automatically starts the generation of the video signal on the analog video output connector.

## **Editing Video Parameters**

You can use the NI Video Generator Wizard to control different video parameters of the video signal.



**Note** Parameters is the informal name for video signal conditions that you can modify through the NI Video Generator Wizard. The term attribute is used in this help file instead of the term parameters.



**Note** To access file options, select **Load BMP file and compute video data** in the NI Video Generator Wizard dialog box.

To edit the video parameters of the video signal, select one of the following options from the NI Video Generator Wizard dialog box:

- Appearance
- <u>Sub-Carrier & Sync</u>
- Filters & Levels
- <u>Test Lines</u>
- <u>Misc.</u>

## **Edit Factory Settings**

When you select Edit factory settings, you access most of the editable video parameters. If you edit and then save the edited video parameters, the NI Video Generator Wizard generates a configuration file. The configuration file stores the edited video parameters, along with other attribute information, and uses these attributes to generate the video signal. To edit these video parameters, complete the following steps:

- 1. Select Edit factory settings.
- 2. On the right side of the dialog box, select **M-NTSC**, **Standard-PAL**, or **SECAM**, depending on the video format you want to generate.
- 3. Select Download video data file.
- 4. Click Next.
- 5. Select the video parameters you want to modify.

### Appearance

The Appearance tab displays the controls for the parameters of the video signal that affect the appearance of the image. For example, you can modify the geometry, such as size and position, and you can modify intensity such as brightness, contrast, or saturation.

The following figure shows the Appearance tab.

🔁 Video Generator Wizard	
M-NTSC	
Appearance Sub-Carrier & Sync.	Filters & Levels   Test Lines   Misc.
Brightness (IRE) ∰0.00	Input Image Width (Pixels)
Contrast Factor	Input Image Heigth (Pixels) 480
Saturation Factor	Image Start Line
Setup Level (IRE)	Image Start Position (μs) 9.50
Tint Correction (degrees) ∰ 0.00	Image Duration (με)
Save Save As	<< Back Finish

### Sub-Carrier & Sync.

The Sub-Carrier & Sync tab displays the controls for the parameters that control the positioning and level of the composite synchronization pulses and color burst signals.

The following figure shows the Sub-Carrier & Sync tab.



### **Filters & Levels**

The Filters & Levels tab displays the controls for the output level and offset of the video signal and the filter options that can be applied to the video components.



**Note** NI does not recommended changing the default values for the IRE to ARB Gain and IRE to ARB Offset parameters. The default values are optimized for best dynamic results of the source.

The following figure shows the Filters & Levels tab.

Nideo Generator Wizard	
M-NTSC	
Appearance Sub-Carrier & Sync.	Filters & Levels Test Lines Misc.
IRE to ARB Gain 250.00 IRE to ARB Offset -4000 mV / IRE 7.143 Zero at Blanking	Composite Filter Gff Y Filter Gff I Filter I .3 MHz FIR Q Filter 0.4 MHz IIR
Save Save As	<< Back Finish
### **Test Lines**

In the Test Lines tab you can define a list of insertion test signals (ITS) to be inserted on specific lines in the video signal. Use the New, Duplicate, Edit, or Delete buttons to complete the following tasks:

- Create a new set of lines
- Duplicate or edit an existing set of lines
- Delete a previously defined set of lines

The following figure shows the Test Lines tab.

🔁 Video Generato	r Wizard			
M-NTSC			<b>PINS</b>	TIONAL TRUMENTS
Appearance	Sub-Carrier & Sync.	Filters & Levels	Test Lines	Misc.
Test Lines (017017) (018018) (280 282)	(001) M-NTSC NTC (001) M-NTSC color (003) M-NTSC color	-7 composite test sig bars 100-75.its purst its	nal	
	,,		D	New uplicate Edit
			¥	Delete
Save S.	ave As		<< Back	Finish

When you create a new set or edit an existing set of lines, a New Test Lines dialog box appears. Complete the following steps:

- 1. Click **Browse**, and double-click the .its file that you want to use, based on the video format you chose in <u>step 2</u>, or enter the test line file path in **Test Line File Path**.
- 2. In Start Line, specify the start line number where the first test line is expected to appear in the video signal.
- 3. In Number of Lines, specify the total number of consecutive lines you want to generate.
- 4. Click **OK** to add or modify the set of test lines to the list, or click **Cancel** if you do not want to apply these changes.



**Note** Due to the interlaced nature of the video signal, a defined set of test lines is inserted in only one field of the video signal. If you want the same set of lines to also be inserted in the other field, click **Duplicate**, then click **Edit**, and change the start line number to the value corresponding to the other field. For example, to duplicate lines from the odd field to the even field, add 263 (for M-NTSC or M-PAL formats) or 313 (for all other formats) to the actual start line value.

### Misc.

The Misc. tab displays the controls for a few miscellaneous parameters that you can modify in the video signal. You can add optional harmonic distortion to the chroma signal using Chroma Second Harmonic (%) and Chroma Third Harmonic (%), or you can add white noise to the composite video signal using Noise Level (IRE rms).

The following figure shows the Misc. tab.

🔁 Video Generator Wizard						
M-NTSC						
Appearance Sub-Carrier & Sync.	Filters & Levels Test Lines Misc.					
Noise Level (IRE rms) 0.00 Chroma Second Harmonic (% 0.00 Chroma Third Harmonic (%)	Digital Sync Pattern					
Save Save As	< Back Finish					

To save the edited settings, complete the following steps:

- 1. Click either **Save** or **Save As** to save the edited configuration, which includes the edited video parameters, the video format you selected, and so on.
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- **Note** If you click **Save As**, enter the edited configuration file name, such as My_config.cfg.
- 2. Click **Finish**. A Processing dialog box appears showing the processing status.

The NI Video Generator Wizard calculates a new binary video data file based on the edited configuration, downloads it to the NI PXI/PCI-5431, then starts the generation of the video signal on the analog video output connector. This binary file is not saved.

# **Use Custom Settings**

When you select **Use custom settings**, you can recall any previously customized and saved configuration file and apply these settings to a video signal based on any bitmap image that you select in the Video Generator Wizard dialog box. Several customized configuration files are already installed on the computer. The configuration file that you recall contains only the video parameters, video format, and so on, but does not refer to a specific bitmap image.

To generate a video signal using previously defined custom settings, complete the following steps:

- 1. Select **Use custom settings** from the Video Generation Wizard. In the Settings File Path, an example file called NTSC low saturation.cfg is already selected. This configuration file results in the generation of a video signal with half the normal saturation level that is an image with weak colors.
- 2. To select any other configuration files, such as PAL low saturation.cfg or SECAM low saturation.cfg, complete the following steps:
  - a. Navigate to the .cfg file you want to apply to the video signal.
  - b. Double-click the file.
- 3. Select Download video data file.
- 4. Click **Finish.** A Processing dialog box appears showing the processing status.

A new video signal based on the selected configuration computes and downloads to the NI 5431.

# **Editing Custom Settings**

When you select **Edit Custom Settings**, you can recall and edit a previously customized and saved configuration file that you created using Edit Factory Settings or that the installation CD installed in the computer. To recall and edit a configuration file, complete the following steps:

- 1. Click **Browse** to search for the .cfg file you want to edit.
- 2. Double-click the .cfg file you want to edit.
- 3. Click **Next** to access the video parameters you want to edit.
- 4. Select the video parameters you want to modify in any of the five displayed tabs.
- 5. Save the configuration you edited using either Save or Save As.
  - a. Enter the new name of the edited .cfg file, if necessary.
  - b. Click **Save** to save the edited .cfg file in the Configuration files directory.
- 6. Click **Finish**. A Processing dialog box appears showing the processing status.

A new video signal based on the edited configuration is computed and downloaded to the NI PXI/PCI-5431.

## NI Video Generator Wizard: Downloading and Saving a Video Data File

To download the calculated video data for the video signal to the NI PXI/PCI-5431, or to save this data to disk, select one of three options found in the bottom section of the NI Video Generator Wizard dialog box:

- Download video data file
- Save video data file to disk
- Save and download
- Note Select Load BMP file and compute video data to access options.

## NI Video Generator Wizard: Downloading Video Data File

The Download video data file command downloads the binary video data file to the NI PXI/PCI-5431 based on the bitmap image selected in BMP Input File Path and the video settings you selected in the NI Video Generator Wizard. The NI Video Generator Wizard does not save this downloaded binary video data file.

If you select Use factory settings, refer to <u>Generating a Video Signal</u> for more information. If you select Use custom settings, refer to <u>Using</u> <u>Custom Settings</u> for more information.

# Saving Video Data File to Disk

Save Video Data File to Disk generates and saves a binary video data file to disk. This binary video data file is the result of the calculation based on the bitmap image selected in the BMP Input File Path and video settings selected in the NI Video Generator Wizard dialog box.

To save a binary video data file to disk, complete the following steps:

- 1. If you select **Use factory settings**, refer to <u>Generating a Video</u> <u>Signal</u> and follow steps 1-7. If you select **Use custom settings**, refer to <u>Using Custom Settings</u> and follow steps 1-2.
- 2. Select **Save video data file to disk**, NI Video Generator Wizard dialog box. The Save As dialog box appears.
- 3. Based on the video format you chose, double-click a directory to save the new binary video data file in.
  - Note You can also enter the path where you want to save the binary video data file in the Video Output File Path field, such as in the Video data files directory.
- 4. Enter a name for the binary video data file, such as my_bin.bin.
- 5. Click **Save**. A Processing dialog box appears showing the processing status.

A new binary video data file is saved to disk.



**Note** After the binary video data file is saved, you can select Load Video Data File from Disk in the **NI Video Generator Wizard** dialog box to generate a video signal directly from the binary video data file. Refer to <u>Loading Video Data File from Disk</u> for more information about using a binary video data file to generate a video signal.

# Saving and Downloading

Save and Download combines the Download Video Data File and Save Video Data File to Disk commands. This option generates and saves a binary video data file to disk, downloads it to the NI PXI/PCI-5431, then starts generation.

# Loading Video Data File from Disk

When you select **Load video data file from disk**, the middle section of the dialog box changes as shown in the following figure.

🔁 Video Generator Wizard	
<ul> <li>Load video data file from disk</li> <li>Load BMP file and compute video data</li> <li>BMP Input File Path</li> <li>C:\Program Files\National Instruments\NI-vid</li> </ul>	Browse Display BMP Device ID # 1
<ul> <li>Use factory settings</li> <li>Use custom settings</li> <li>Edit factory settings</li> <li>Edit custom settings</li> </ul>	<ul> <li>M-NTSC</li> <li>Standard PAL</li> <li>M-PAL</li> <li>N-PAL</li> <li>Combination N-PAL</li> <li>SECAM</li> </ul>
<ul> <li>Download video data file</li> <li>Save video data file to disk</li> <li>Save and Download</li> </ul>	Exit Finish

Load video data file from disk downloads a previously saved binary video data file to the NI PXI/PCI-5431 and starts generation of the video signal on its video output connector.

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**Note** Only an experienced user should alter the Used IRE to ARB Gain and Used IRE to ARB Offset settings. These settings affect the signal levels generated by the hardware. The values in these controls should match the values used when the video data file was created and saved. Refer to <u>Saving Video Data File to Disk</u>.

To generate a video signal using the Load Video Data from Disk option, complete the following steps:

- 1. Select Load video data file from disk.
- 2. Using the Browse button, double-click any binary video data file to download from the Video data files directory, such as my_bin.bin, which you generated and saved in <u>Save Video Data File to Disk</u>.
- 3. In the middle section of the dialog box, make sure you select the correct value in the Output level that corresponds to the video

format previously incorporated into the binary video data file. The nominal value is 7.143 mV/IRE for M-NTSC, M-PAL, and N-PAL, and 7.000 mV/IRE for all other video formats, as shown in the bottom section of the dialog box.

4. Click **Finish**. A Downloading dialog box appears, showing the progress of the download. As soon as the dialog box disappears, the video signal should be generated by the NI 5431.

# Programming

Expand this topic for information about programming with NI-FGEN and NI Composite Video Generator.

## NI-FGEN Instrument Driver Overview

To create your application, you need an industry-standard instrument driver such as NI-FGEN to control your device. NI-FGEN is IVI-compliant and works with NI LabVIEW, NI LabWindows/CVI, and conventional programming languages such as Microsoft Visual C, C++, and Visual Basic.

NI-FGEN includes a set of standard functions for configuring, creating, starting, and stopping waveform generation. NI-FGEN reduces your program development time and simplifies device control by eliminating the need to learn a complex programming protocol for your device.

Refer to the <u>NI-FGEN Instrument Driver Readme</u> for more information. You can access this document by selecting **Start**»All **Programs**»National Instruments»NI-FGEN»Documentation.

## NI-FGEN Programming State Model

In this topic the word "property," when not referring to a specific property, refers to both properties in LabVIEW and attributes in C or CVI.

The NI-FGEN programming model has three main states: Idle, Committed, and Generating, as shown in the following figure.



**Idle**–You can program all session properties in the Idle state. However, when in the Idle state, the properties may not have been applied to the device yet, so the device hardware configuration may not match the session property values–the device remains configured as it was the last time a session was committed. If the computer has just been reset or the niFgen Reset Device VI or the niFgen_ResetDevice function has just been called, the device is in the default hardware state. This means the device is not generating a waveform, although, depending on the previous state, a constant DC voltage from the last waveform sample generated on the output connector may be present.

**Committed**–All of the session properties are applied to the device when the session enters the Committed state. In the Committed state, waveforms and sequences can be loaded into onboard memory. If any properties are changed, the session implicitly transitions back to idle, and the hardware configuration still reflects the previously committed properties. Calling the niFgen Commit VI or the niFgen_Commit function from the Idle state verifies all properties, configures the device, and transitions to the Committed state. **Generating**–In the Generating state, session properties always reflect the current state of the device, and the device is either waiting on a trigger or generating a signal. Dynamic properties, such as the <u>Arbitrary</u> <u>Waveform Gain</u> property or the <u>NIFGEN_ATTR_ARB_GAIN</u> attribute and the <u>Arbitrary Waveform Offset</u> property or the <u>NIECEN_ATTR_ARB_OFFSET</u> attribute, are applied to the device

<u>NIFGEN_ATTR_ARB_OFFSET</u> attribute, are applied to the device immediately if set while the session is in the Generating state.

The following actions or settings cause a transition from one state to another:

- Calling the <u>niFgen Initiate Generation</u> VI or the <u>niFgen_InitiateGeneration</u> function in the Idle state causes a transition to the Generating state.
- Calling the <u>niFgen Commit</u> VI or the <u>niFgen_Commit</u> function in the Idle state causes a transition to the Committed state.
- Calling the any create or write waveform VI or function in the Idle state causes a transition to the Committed state.
- Calling the <u>niFgen Create Arbitrary Sequence</u> VI or the <u>niFgen_CreateArbSequencee</u> function, or the <u>niFgen Create</u> <u>Advanced Arb Sequence</u> VI or the <u>niFgen_CreateAdvancedArbSequence</u> function in the Idle state causes a transition to the Committed state.
- Changing any property in the Committed state causes a transition to the Idle state.
- Changing a property that is not dynamic in the Generating state returns an error, but does not transition out of the Generating state.
- Calling the <u>niFgen Abort Generation</u> VI or the <u>niFgen_AbortGeneration</u> function in the Generating state causes a transition to the Committed state.
- Calling the <u>niFgen Close</u> VI or the <u>niFgen_close</u> function from any state closes the NI-FGEN session and transitions to the close state. If the session is in the Generating state, the generation is aborted first.
- Calling the <u>niFgen Reset</u> VI or the <u>niFgen_reset</u> function from any state causes a transition to the Idle state. If the session is in the Generating state, the generation is aborted first.

### NI-FGEN General Programming Flow

The following diagram shows the general programming flow for applications using NI-FGEN. Not all NI-FGEN VIs appear in the general programming flow as some VIs are considered utility VIs, which perform tasks such as resetting the device and returning the revision number of NI-FGEN. Refer to the <u>NI-FGEN LabVIEW Reference</u> or the <u>NI-FGEN C</u> <u>Function Reference</u> for more information.



# **Simulation Mode**

NI signal generators support simulation. Simulating a device enables you to perform the following tasks:

- Protect your devices by first testing settings and configurations on simulated devices.
- Verify device behaviors under a wide variety of operating conditions.
- Start or speed up application development before you have the hardware.
- Optimize designs and determine ideal design parameters.

Enabling simulation allows you to verify that you have correctly configured the device. For example, if a parameter is set to an invalid value for the device, NI-FGEN returns the same error it would for a real device. While simulation is useful for verifying your configuration, there are some areas where simulation is not sufficient to verify that your configuration is correct. For example, no errors will be returned for configurations that involve or depend upon external signals, such as configuring an external Sample clock or routing signals. Also, the amount of time a generation takes to complete will be ignored in simulation mode; a finite generation will finish immediately after it is initiated, regardless of how much data is downloaded and how fast it is generated.

### Simulation in LabVIEW

In LabVIEW, simulation is enabled with the Option String parameter of the niFgen Initialize With Options VI. Enable simulation (Simulate=1) and specify the device you want to simulate with the option string input.

The following example enables simulation of the NI PCI-5421 with 256 MB of onboard memory:



For more information, see the <u>niFgen Initialize With Options VI</u>.

### Simulation in LabWindows/CVI

In LabWindows/CVI, simulation is enabled with the niFgen_InitWithOptions function. Enable simulation (Simulate=1) and specify the device you want to simulate with the option string parameter.

The following example enables simulation of the NI PCI-5421 with 256 MB of onboard memory:

niFgen_InitWithOptions (Resource, VI_ON, VI_ON, "Simulate=1, DriverSetup=Model:5421;BoardType:PCI;MemorySize:268435456",&vi );

For more information, see the <u>niFgen_InitWithOptions</u> function.

## **NI-FGEN Error Codes**

When the NI-FGEN driver encounters an error, it returns an error code. This code value can be in hexadecimal, decimal, or text depending on your application. To understand the error code, you need to read the error description.

For example, the error "-1074135039" or "(0xBFFA0001 - Instrument Specific error)" encompasses many different error cases. To better understand the error specific to your application, you need to read the error description.

### **Reading Error Descriptions in LabVIEW**

LabVIEW users can read the error description by creating an error indicator from one of the NI-FGEN VIs as shown in the following figure.



### **Reading Error Descriptions in CVI and C**

CVI and C users can read the error description by calling the <u>niFgen_GetError</u> function.

## NI-FGEN Creating an Application with NI-FGEN and Your ADE

This topic covers how to begin using NI-FGEN with your application development environment (ADE) and lists any files that you need to include in your application.

To successfully build your application, you need to have NI-FGEN installed, along with one of the following ADEs:

- <u>NI LabVIEW</u>
- NI LabVIEW Real-Time
- <u>NI LabWindows/CVI</u>
- <u>Microsoft Visual C/C++</u>
- <u>Microsoft Visual Basic</u>

# NI-FGEN Creating an Application with LabVIEW

This topic assumes that you are using LabVIEW to manage your code development and that you are familiar with the ADE.

To develop an NI-FGEN application in LabVIEW, follow these general steps:

- 1. Open an existing or new LabVIEW VI.
- 2. From the Function palette, locate the NI-FGEN VIs at **Instrument I/O**»Instrument Drivers»NI-FGEN.
- 3. Click the Vis that you want to use, and drop them on the block diagram to build your application.

#### **NI-FGEN Example Programs for LabVIEW**

If you are using LabVIEW 7.0 or later, you can use the NI Example Finder to search or browse examples. NI-FGEN examples are classified by keyword, so you can search for a particular device or measurement function.

To browse the NI-FGEN examples available in LabVIEW, launch LabVIEW, click **Find Examples**, and navigate to **Hardware Input and Output»Modular Instruments»NI-FGEN**.

For the installation location of the LabVIEW example files, refer to the <u>NI-FGEN Instrument Driver Readme</u>.

### **Considerations for using the LabVIEW Real-Time Module**

To develop an NI-FGEN application in the LabVIEW Real-Time Module, follow the same steps used for developing any application in the LabVIEW Real-Time Module, with the addition of using the NI-FGEN LabVIEW VIs.

#### Supported LabVIEW Versions

LabVIEW Real-Time Module 7.1 or later

#### **Unsupported Hardware**

The following signal generators are not supported as targets for your LabVIEW RT application:

- NI PXI/PCI-5401
- NI PXI/PCI-5411
- NI PXI/PCI-5431

#### **Unsupported Features**

When using the National Instruments signal generators with LabVIEW RT, the following features are *not* supported:

- External calibration
- Express VIs
- FGEN Soft Front Panel

#### **Related Documentation**

- For configuration instructions for remote systems, refer to the *MAX Remote Systems Help* in Measurement & Automation Explorer (MAX) by selecting **Help*Help Topics*Remote Systems** in MAX.
- For more information about the LabVIEW Real-Time Module, refer to the *LabVIEW Real-Time Module User Manual* at <u>ni.com/manuals</u>.
- For additional troubleshooting and support information, refer to the LabVIEW Real-Time Support main page at <u>ni.com/support/labview/real-time</u>.

# NI-FGEN Creating an Application with LabWindows/CVI

This topic assumes that you are using LabWindows/CVI to manage your code development and that you are familiar with the ADE.

To develop an NI-FGEN application in LabWindows/CVI, follow these general steps:

- 1. Open an existing or new project file.
- 2. Load the NI-FGEN function tree (niFgen.fp) from VXIPnP\ <WinNT|9x>\niFgen.
- 3. Use the function tree to navigate the function hierarchy and to generate function calls with the proper syntax and variable values.

#### **NI-FGEN Example Programs for LabWindows/CVI**

To locate the example programs installed with NI-FGEN, refer to the <u>NI-FGEN Instrument Driver Readme</u>.

If you are using LabWindows/CVI 7.0 or later, you can use the NI Example Finder to search or browse examples. NI-FGEN examples are classified by keyword, so you can search for a particular device or measurement function.

To browse the NI-FGEN examples available in LabWindows/CVI, launch LabWindows/CVI, select **Help»Find Examples**, and navigate to **Hardware Input and Output»Modular Instruments»NI-FGEN**. You can also access the examples using the Start menu, by selecting **Start»All Programs»National Instruments»NI-FGEN»Examples**.

# NI-FGEN Creating an Application with Visual C/C++

This topic assumes that you are using Visual C/C++ to manage your code development and that you are familiar with the ADE.

To develop an NI-FGEN application in Visual C/C++, follow these general steps:

- 1. Open an existing or new Visual C/C++ project.
- Create source files—.c (C source code) or .cpp (C++ source code) and add them to the project. Make sure that you include the NI-FGEN header file (niFGEN.h) in your source code files as follows: #include "niFGEN.h"
- Specify the directory that contains the NI-FGEN header file under the Preprocessor»Additional include directories settings in your compiler–for Visual C++ 6.0 these files are under Project»Settings»C/C++. For the location of the NI-FGEN header files, refer to the NI-FGEN Instrument Driver Readme.
- Add the NI-FGEN import library (niFGEN.lib) to the project under Link»General»Object/Library Modules. For the location of the NI-FGEN import library files, refer to the <u>NI-FGEN Instrument</u> <u>Driver Readme</u>.
- 5. Add NI-FGEN function calls to your application.
- 6. Build your application.

#### NI-FGEN Example Programs for Visual C/C++

To locate the example programs installed with NI-FGEN, refer to the <u>NI-FGEN Instrument Driver Readme</u>.

#### **Special Considerations**

#### **String Passing**

To pass strings, pass a pointer to the first element of the character array. Be sure that the string is null-terminated.

#### **Parameter Passing**

By default, Visual C passes parameters by value. Remember to pass pointers to variables when you need to pass by address.

# NI-FGEN Creating an Application with Visual Basic

This topic assumes that you are using Visual Basic to manage your code development and that you are familiar with the ADE.

To develop an NI-FGEN application in Visual Basic, follow these general steps:

- 1. Open an existing or new Visual Basic project.
- 2. Create the following files, which are necessary for your application, and add them to your project:
  - .frm (form definition and event handling code)
  - (optional) .bas (Visual Basic generic code module)
  - (optional) .cls (Visual Basic class module)
- 3. Add a reference to the National Instruments Function Generator library (NI-FGEN), which is part of niFgen_32.dll by selecting **Project**»References, and then National Instruments Function Generator.
  - Note If you do not see the NI-FGEN library listed there, click **Browse** and locate niFGEN_32.dll in the directory listed in the <u>NI-FGEN Instrument Driver Readme</u>.
- 4. Use the Object Browser <F2> to find function prototypes and constants.
- 5. Add NI-FGEN function calls to your application.
- 6. Run your application by clicking **Run»Start**.

## **NI-FGEN Visual C++ Reference Help**

For help with NI-FGEN methods and properties, refer to the *NI-FGEN Visual C++ Instrument Driver Overview* included in the *NI Measurement Studio Help.* 

You can access the NI Measurement Studio Help in the following ways:

- From the Windows Start menu, select **Start»Programs»National Instruments»Measurement Studio 7.0»<Measurement Studio Documentation>**. The help launches in a stand-alone help viewer.
- From Visual Studio .NET, select **Help»Contents** to view the Visual Studio .NET table of contents. The *NI Measurement Studio Help* is listed in the table of contents.

## NI-FGEN Examples for Measurement Studio

NI-FGEN ships with several examples for use with Measurement Studio. These examples can help you develop software, and they illustrate how to perform the most common operations with the NI signal generators.

### **Microsoft Visual Basic 6.0 Examples**

These examples provide an overview for using NI-FGEN in Visual Basic.

To use an example in Visual Basic, open the project file (.vbp) of the example you want to run. For the installation locations of the project files, Refer to the <u>NI-FGEN Instrument Driver Readme</u>.

When developing applications with Visual Basic and NI-FGEN, you must include the NI arbitrary waveform and function generator library as one of the references for the project. To select the NI Function Generator library from Visual Basic, select **Project**»**References**, and then select **National Instruments Function Generator**. If the reference is not already listed, you can add the reference by browsing and selecting the niFgen_32.dll in the directory specified in the <u>NI-FGEN Instrument Driver Readme</u>.

### **Microsoft Visual C++ 6.0 Examples**

To use an example, open the workspace (.dsw) of the example you want to run. Refer to the <u>NI-FGEN Instrument Driver Readme</u> for the location of the example files. Build the example. The executable is created in the \debug directory of the respective example.

The source code for these examples is documented, as well as all of the input and output values, to make changing the code to perform different types of generation easier.

### Microsoft Visual C++ .NET 2003 Examples

To use an example, open the solution file (.sln) of the example you want to run. Refer to the <u>NI-FGEN Instrument Driver Readme</u> for the location of the example files. Build the example. The executable is created in the \debug directory of the respective example.

The source code for these examples is documented, as well as all of the input and output values, to make changing the code to perform different types of generation easier.

## How the NI Video Software Toolkit Filters Video Components

The NI Video Software Toolkit has several ways to filter different video components while computing a video signal. The video formats PAL, NTSC, and SECAM require some of the filters, while other filters are optional. Three filtering modes exist:

- One or more of the predefined FIR filters
- One or more of the predefined IIR filters
- One or more user-defined FIR or IIR filters. Refer to the <u>Advanced</u> <u>Color Bars from ITS with Custom Filters</u> example.

Predefined filters do not have a group delay across the entire frequency range. In other words, phase error and delay do not exist between any part of the different signal components, whether these components are filtered or not.



**Note** The IIR filters are not classical-type IIR filters but rather an advanced version of the IIR filtering with symmetrical impulse response, that is, zero group delay error.

The key difference between an FIR and an IIR filter is whether the impulse response is finite (FIR) or infinite (IIR). FIR filtering is faster in computation than IIR filtering and often has a step response with less overshoot than the equivalent IIR filter. On the other hand, the frequency response of the FIR filters is not as sharp as the corresponding IIR filter.

The use of the FIR or IIR filter type depends on the application. If frequency attenuation is important, the IIR filters are recommended. If fast calculation time is a higher priority, then the FIR filters may be a better choice. If you do not specify anything, the video toolkit software uses default filters that fulfill the different requirements of the video standards.

The default filters are as follows:

- For NTSC:
  - Y (luminance component): No filter
  - Q (first chroma component): 0.4 MHz IIR filter
  - I (second chroma component): 1.3 MHz FIR filter

- Entire composite signal: No filter
- For PAL or SECAM:
  - Y (luminance component): No filter
  - U (first chroma component): 1.3 MHz FIR filter
  - V (second chroma component): 1.3 MHz FIR filter
  - Entire composite signal: No filter

The following table lists the filter specifications.

Filter Cut-Off	Designed for Filtering	Filter Type	Attenuation at Cut-Off	Stop-Band Frequency	Attenuation in Stop Band
0.4 MHz	Q component	IIR only	< 2 dB	0.6 MHz	> 6 dB
1.3 MHz	I/U/V component	FIR/IIR	< 2 dB	3.6 MHz	> 20 dB
4.2 MHz	M-NTSC signal	FIR/IIR	3 dB	Refer to following figures	Refer to following figures
5.0 MHz	B/G-PAL signal	FIR/IIR	3 dB	Refer to following figures	Refer to following figures
5.5 MHz	I-PAL signal	FIR/IIR	3 dB	Refer to following figures	Refer to following figures
6.0 MHz	D-PAL signal	FIR/IIR	3 dB	Refer to following figures	Refer to following figures

The following figures show the frequency response for all the predefined FIR and IIR video filters.


**Frequency Response for the Predefined FIR Filters** 



Frequency Response for the Predefined IIR Filters

# **Operating System Support**

For information about the supported operating system (OS) for your device, refer to the <u>NI-FGEN Instrument Driver Readme</u>.



**Note** Some devices are not supported under Windows Vista. Refer to the <u>NI-FGEN Instrument Driver Readme</u> for a complete list of products and their OS support.



#### Prefixes

Symbol	Prefix	Value
р	pico	10-12
n	nano	10 ⁻⁹
μ	micro	10-6
m	milli	10-3
k	kilo	10 ³
М	mega	106
G	giga	10 ⁹
Т	tera	1012

#### Numbers/Symbols

		-
Symbol	Meaning	Value
nV	nanovolts	10 ⁻⁹ V
μV	microvolts	10 ⁻⁶ V
μΩ	microohms	10 ⁻⁶ Ω
mΩ	milliohms	10 ⁻³ Ω
MΩ	megaohms	10 ⁶ Ω
рА	picoamps	10 ⁻¹² A
nA	nanoamps	10 ⁻⁹ A
μΑ	microamps	10 ⁻⁶ A
mA	milliamps	10 ⁻³ A
-		-

### Α

- ADC Analog-to-Digital Converter—An electronic device, often an integrated circuit, that converts an analog voltage to a digital value. Also abbreviated as A/D Converter.
- alias A false lower frequency component that appears in sampled data acquired at too low a sampling rate.

arbitrary Instrument for generating arbitrary video waveform; this instrument is not restricted to standard waveforms such as generator sine or square.

array Ordered, indexed list of data elements of the same type.

attribute Parameter or configuration applied to the video signal.

#### В

- bandwidth The range of frequencies present in a signal, or the range of frequencies to which a measuring device can respond. For signal generators, bandwidth is the frequency at which the amplitude of the frequency response is 3 dB lower than the amplitude of the frequency response at DC or a low frequency.
- .bin File extension for a binary file. See binary file.
- binary file 16-bit file format used to save the data of a complete composite video signal. See .bin.
- bitmap RGB image format. See .bmp.

image

block Optimized calculation mode where a block of video lines is computed simultaneously.

.bmp File extension on a bitmap image. See bitmap image.

С	
С	Chroma component in a composite video signal. See <u>S-</u> <u>Video</u> or <u>Y/C.</u>
.cfg	File extension on a configuration file. See configuration file.
chroma	The color part of the video signal in the M-NTSC and PAL video signal.
composite Iuma	A monochrome composite video signal. See $\underline{Y}$ .
composite video signal	A single signal that contains color video and timing information.
configuration file	A file where you can save your specific video signal setup conditions such as the video parameters or attributes, video format, and some other information regarding the signal.
Csync	Composite synchronization signal; a single signal including both horizontal and vertical synchronization pulses.

D
υ

DAC	Digital-to-Analog Converter—An electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current.
data marker event	An event that allows you to export any one of the waveform data bits to any valid destination on the device.
DDS	direct digital synthesis—A signal generation technique giving very high-frequency resolution.
digital synchronization	Digital TTL signals delivering Csync, Vsync, Hsync, and field ID signals.
DMM	Digital MultimeterA digital instrument capable of measuring several different fundamental electrical characteristics, most often voltage, resistance, and current.

#### Ε

ENOB Effective Number of Bits—A way of specifying the signal-tonoise-and-distortion ratio (see <u>SINAD</u>) that indicates how close a DAC is to an ideal DAC of the same size.

FCW	Frequency Control Word—The phase accumulator is incremented by the value of the FCW to generate the desired frequency of the output signal.
field ID	Signal that identifies the even or odd field in an interlaced video frame.
filter coefficients	Constant values that characterize a digital filter.
filter data	See filter coefficients.
filters	Digital or analog circuits that change the frequency characteristics of a video signal.
frequency modulation sub-carrier	Carrier signal in SECAM used to represent the chroma information.

#### G

gain Amplification of a signal. A gain of two corresponds to a doubling of the signal level.

## Н

high-level Hardware dependent VI that simplifies the needed

- driver VI programming. All high-level drivers are based on low-level Vis.
- Hsync Horizontal sync—the portion of the video signal that tells the display where to put the picture in the left-to-right dimension. See horizontal sync pulse.

horizontal Pulse that controls line-by-line scanning. sync

Syric

pulse

## I

insertion Test signals to be inserted on specific lines either in the vertical blanking interval or in the active image region.
signals
IRE Unit used to describe the level of a video signal. Pure white is defined as 100 IRE. The blanking level is defined as 0 IRE.
ITS Insertion Test Signals

## L

line-by- Calculation mode where the video lines are computed one at line mode a time.

least The four bits present in the 16-bit data word that are not used significant to represent the analog signal. These bits contain the digital bits synchronization signals.

lookup Fixed-size memory that stores one cycle of a periodic memory waveform.

looping Repeating the same buffer in the waveform memory. This method of waveform generation decreases memory requirements.

low-level The lowest level of programming. The low-level driver VIs

- driver VI offer the most functionality but require more programming.
- Isbs See least significant bits.
- luma The monochrome part of the composite video signal.

## Μ

maps	A bitmap image needs to be mapped by the software before it is used to compute a composite video signal.
marker event	An event that the device generates in relation to a waveform that is generated. The event is configured to occur at the time that a specific location or sample $n$ in the waveform generates on the CH 0 connector.
modulation cosine	Cosine function representing the sub-carrier for the second chroma component in PAL or NTSC systems.
modulation sine	Sine function representing the sub-carrier for the first chroma component in PAL or NTSC systems.
M-NTSC	see <u>NTSC</u> .
M-PAL	Video standard used in Brazil. Uses 525 lines per frame.

#### Ν

- NI 5431 NI PXI/PCI-5431 video signal generator. See <u>NI 5431</u> <u>Composite Video Generator</u>.
- N-PAL Video standard used in Argentina. Uses 625 lines per frame.
- NTSC(M- National Television Standards Committee; the video standard
- NTSC) used in North America and Japan. Uses 525 lines per frame.

#### 0

offset Constant value added to a signal.

OSP onboard signal processing

#### Ρ

PAL	Phase Alternation Line—color video standard used in Europe and in many other countries outside the US M-PAL uses 525 lines per frame. All other PAL formats use 625 lines per frame.
parameters	Non–programmer's term for video signal conditions that you can modify using the NI-VDG.dll. See <u>attribute</u> .
passband	The range of frequencies which a device can properly propagate or measure.
passband flatness	A measure of the amplitude accuracy of the frequency response with respect to frequency. Passband flatness is typically specified in $\pm$ dB and referenced to the amplitude of the frequency response at a designated frequency.
PLL	phase-locked loop—An electronic circuit which forces an output frequency to be locked to the same phase as a reference frequency.
prepare mode	Mode to be called before lines calculation in block mode.

#### R

release Mode to be called after lines calculation in block mode.

- resolution The smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244 percent of full scale.
- RGB red, green, blue
- RGB ITS Three data arrays (R, G, and B) of unsigned 16-bit data (U16).
- rms root-mean-squareThe square root of the average value of the square of the instantaneous signal amplitude; a measure of signal amplitude. The rms voltage of a signal is computed by squaring the instantaneous voltage, integrating over the desired time, and taking the square root.

## S

sample rate	The rate at which digital data is transferred from the memory to the DAC.
saturation factor	The amount of color pigment present. The less saturated a color is, the more white that is present in the color.
scaling	The act of changing the effective resolution of an image.
script	A series of instructions that indicates how waveforms saved in the onboard memory should be sent to the device under test.
SECAM	Sequential Couleur Avec Memoire or Sequential Color with Memory. Video standard used in France and parts of Africa and Middle East. Uses 625 lines per frame. In SECAM, the chroma is FM modulated and the R'-Y and B'-Y signals are transmitted line sequentially.
settings	Video signal conditions, which are also knows as video parameters or attributes.
SFDR	spurious-free dynamic rangeThe dynamic range from full- scale deflection to the highest spurious signal in the frequency domain.
SGL	single precision
signed 16-bit values	16-bit integer values in the range [–32,768 to +32,767].
SINAD	Signal-to-Noise-and-Distortion ratio—ratio of the rms signal amplitude to the rms sum of all other spectral components, including the harmonics, but excluding DC.
S-Video	see Y/C
sync	Synchronization signals controlling the horizontal and vertical deflections in a TV.

## Т

- THD total harmonic distortion—The ratio of the total rms signal due to harmonic distortion to the overall rms signal, in dB or percent.
- transient A brief oscillation resulting from a sudden change of voltage, current, or load.
- trigger Signal that causes the NI device to perform an action such as starting or stopping a generation operation.
- TTL Transistor-Transistor Logic

unmap The bitmap image is unmapped after being used to compute a composite video signal.

U

#### V

VCXO	voltage-controlled crystal oscillator
vertical sync pulses	Pulses that control the vertical scanning. See Vsync.
video attribute	A parameter of a video signal.
video data file	File containing the binary data that represent a video signal.
video format	Specifies the video norm used to compute the video signal such as M-NTSC or SECAM.
video lines	The lines that compose a video signal.
NI 5431 Composite Video Generator	The software package from your installation CD, which takes care of the needed calculations and driver functions especially developed to interface between your computer and your NI 5431.
video waveform	What the signal looks like to the video output device.
Vsync	Vertical sync; the portion of the video signal that tells the display where to place the image in the top-to-bottom dimension. See vertical sync pulses.

## Y

- Y Luma component in a composite video signal. See <u>S-Video</u> or Y/C.
- Y/C Video signal where the luma signal Y and the chroma signal C are distributed independently.
- YIQ Color space used in the M-NTSC color system. Y represents the luma component while I and Q are the two color difference components.
- YUV Color space used by the PAL color system. Y is the luma component while U and V are the two color difference components.

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# **Direct DMA**

Direct DMA can transfer waveform data to the signal generator onboard memory at rates well beyond the typical 5 to 30 MB/s range in a standard PC-based architecture. To achieve such high rates, direct DMA establishes a direct connection between the signal generator onboard memory and a specialized waveform data source. Direct DMA is commonly used to <u>stream</u> waveform data from disk at data rates of 100+ MB/sec. Conduant's StreamStor[™] products are one example of direct DMA-compatible data sources.
## **Configuring Your Application for Direct DMA**

The following instructions are a guide for configuring your application for direct DMA.

- Enable the signal generator for direct DMA writes by setting the <u>Direct DMA Enabled</u> property or the <u>NIFGEN_ATTR_DIRECT_DMA_ENABLED</u> attribute. Once enabled, NI-FGEN monitors and reports any issues with the direct DMA transfer.
- Identify the waveform data source and set the <u>Direct DMA</u> <u>Window Address</u> property or the <u>NIFGEN_ATTR_DIRECT_DMA_WINDOW_ADDRESS</u> attribute to the address provided by your direct DMA-compatible data source.
- 3. Set the <u>Direct DMA Window Size</u> property or the <u>NIFGEN_ATTR_DIRECT_DMA_WINDOW_SIZE</u> attribute to the size of the memory window provided by your direct DMA-compatible data source.
- 4. Use the <u>niFgen Write Waveform I16 Direct DMA</u> VI or the <u>niFgen_WriteBinary16Waveform</u> function to write blocks of data to the signal generator. For each block of data written to the signal generator, you provide the address of the direct DMA window instead of an array of samples residing in host memory. NI-FGEN detects when the address is within the direct DMA window and handles the transfer appropriately.

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