NI R Series Reference and Procedures

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Use this book for information about which FPGA device I/O functions, terminals, arbitration options, methods, and properties each NI R Series device supports. This book also provides instructions for using LabVIEW and the LabVIEW FPGA Module with NI R Series devices.

To view related topics, click the **Locate** button, shown at left, in the toolbar at the top of this window. The *LabVIEW Help* highlights this topic in the **Contents** tab so you can navigate the related topics.

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NI R Series Related Documentation

Most R Series manuals are available as PDFs. You must have Adobe Reader with Search and Accessibility 5.0.5 or later installed to view the PDFs. Refer to the <u>Adobe Systems Incorporated Web site</u> at www.adobe.com to download Adobe Reader. Refer to the <u>National</u> <u>Instruments Product Manuals Library</u> at ni.com/manuals for updated documentation resources.

The following documents contain information that you may find helpful as you use this help file:

- <u>Getting Started with R Series Intelligent DAQ</u>—Use this document when installing the software and hardware.
- <u>NI R Series Intelligent DAQ User Manual</u>—Use this manual to learn more about your NI 781*x*R/783*x*R/784*x*R/785*x*R Digital R Series hardware, such as connecting I/O signals to your device.
- <u>NI R Series Intelligent DAQ Specifications</u>—Use this document as a reference for the hardware specifications of the NI 781*x*R/783*x*R/784*x*R/785*x*R Digital R Series device.
- <u>NI 78xxR Utilities Help</u>—Use this help file to learn more about the utilities you can use with your NI 78xxR Multifunction R Series device.

These manuals are also available at **Start»All Programs»National Instruments»NI-RIO**.

NI PCI-7811R Reference

R Series Reconfigurable I/O for PCI (DIO) 160 DIO lines, 1 million gate FPGA

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description
Connector <i>x</i> /DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to access this channel.
Connector <i>x</i> /DIOPORTy	Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of eight digital channels. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this port.
RTSI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data Enable</u> method to access this channel.
RTSI/OSC	RTSI oscillator channel. You can use this channel as an additional trigger channel. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data</u> <u>Enable</u> method to access this channel.

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description	
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.	
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.	
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.	
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.	
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.	

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u>.

NI 7811R Digital Port Assignments

You can use an FPGA I/O Node, configured for reading and writing, with the NI 7811R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 0	DIOPORT 2	16 (LSB) through 23
Connector 0	DIOPORT 3	24 (LSB) through 31
Connector 0	DIOPORT 4	32 (LSB) through 39
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39
Connector 2	DIOPORT 0	0 (LSB) through 7
Connector 2	DIOPORT 1	8 (LSB) through 15
Connector 2	DIOPORT 2	16 (LSB) through 23
Connector 2	DIOPORT 3	24 (LSB) through 31
Connector 2	DIOPORT 4	32 (LSB) through 39
Connector 3	DIOPORT 0	0 (LSB) through 7
Connector 3	DIOPORT 1	8 (LSB) through 15
Connector 3	DIOPORT 2	16 (LSB) through 23
Connector 3	DIOPORT 3	24 (LSB) through 31
Connector 3	DIOPORT 4	32 (LSB) through 39

NI PCI-7813R Reference

R Series Reconfigurable I/O for PCI (DIO) 160 DIO lines, 3 million gate FPGA

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description
Connector <i>x</i> /DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to access this channel.
Connector <i>x</i> /DIOPORTy	Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of eight digital channels. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this port.
RTSI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data Enable</u> method to access this channel.
RTSI/OSC	RTSI oscillator channel. You can use this channel as an additional trigger channel. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data</u> <u>Enable</u> method to access this channel.

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description	
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.	
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.	
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.	
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.	
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.	

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/O only.

NI 7813R Digital Port Assignments

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with the NI 7813R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 0	DIOPORT 2	16 (LSB) through 23
Connector 0	DIOPORT 3	24 (LSB) through 31
Connector 0	DIOPORT 4	32 (LSB) through 39
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39
Connector 2	DIOPORT 0	0 (LSB) through 7
Connector 2	DIOPORT 1	8 (LSB) through 15
Connector 2	DIOPORT 2	16 (LSB) through 23
Connector 2	DIOPORT 3	24 (LSB) through 31
Connector 2	DIOPORT 4	32 (LSB) through 39
Connector 3	DIOPORT 0	0 (LSB) through 7
Connector 3	DIOPORT 1	8 (LSB) through 15
Connector 3	DIOPORT 2	16 (LSB) through 23
Connector 3	DIOPORT 3	24 (LSB) through 31
Connector 3	DIOPORT 4	32 (LSB) through 39

NI PCI-7830R Reference

R Series Reconfigurable I/O for PCI (AI, AO, DIO)

4 AI channels, 4 AO channels, 56 DIO lines, 1 million gate FPGA, 200 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.
Connector <i>x</i> /DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.
Connector <i>x</i> /DIOPORT <i>y</i>	Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> channels. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set Data</u> Output or <u>Set Data Enable</u> method to access this port.
RTSI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.
RTSI/OSC	RTSI oscillator channel. You can use this channel as an additional trigger channel. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data</u> <u>Enable</u> method to access this channel.

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description	
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.	
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.	
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.	
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.	
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.	

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/O only.

NI 7830R Digital Port Assignments

You can use an FPGA I/O Node, configured for reading and writing, with the NI 7830R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39

NI PCI-7831R Reference

R Series Reconfigurable I/O for PCI (AI, AO, DIO)

8 AI channels, 8 AO channels, 96 DIO lines, 1 million gate FPGA, 200 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.
Connector <i>x</i> /DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.
Connector <i>x</i> /DIOPORT <i>y</i>	Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> channels. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set Data</u> Output or <u>Set Data Enable</u> method to access this port.
RTSI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.
RTSI/OSC	RTSI oscillator channel. You can use this channel as an additional trigger channel. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data</u> <u>Enable</u> method to access this channel.

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.
Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/O only.

NI PCI-7833R Reference

R Series Reconfigurable I/O for PCI (AI, AO, DIO)

8 AI channels, 8 AO channels, 96 DIO lines, 3 million gate FPGA, 200 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.
Connector <i>x</i> /DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.
Connector <i>x</i> /DIOPORT <i>y</i>	Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> channels. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set Data</u> Output or <u>Set Data Enable</u> method to access this port.
RTSI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.
RTSI/OSC	RTSI oscillator channel. You can use this channel as an additional trigger channel. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data</u> <u>Enable</u> method to access this channel.

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/O only.

NI PXI-7811R Reference

R Series Reconfigurable I/O Module (DIO) 160 DIO lines, 1 million gate FPGA

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description
Connector <i>x</i> /DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.
Connectorx/DIOPORTy	Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> <u>channels</u> . Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data</u> <u>Output</u> or <u>Set Data Enable</u> method to access this port.
PXI/CLK10	 10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an FPGA I/O Node configured for reading to access this channel. Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start»All Programs»National Instruments»NI-RIO.
PXI/LBR <i>x</i>	Local bus right channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to

	access this channel.
PXI/LBLSTAR <i>x</i>	Local bus left channel <i>x</i> , where <i>x</i> is the channel number. If you are using the device in slot two of the PXI chassis, this channel is a star trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data</u> <u>Enable</u> method to access this channel.
PXI/STAR	Star trigger bus. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to access this channel.
	Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction.
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data Enable</u> method to access this channel. Follow the guidelines for <u>using PXI triggers with</u> the LabVIEW FPGA Module.

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u>.

NI PXI-7813R Reference

R Series Reconfigurable I/O Module (DIO) 160 DIO lines, 3 million gate FPGA

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description
Connector <i>x</i> /DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.
Connectorx/DIOPORTy	Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> <u>channels</u> . Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data</u> <u>Output</u> or <u>Set Data Enable</u> method to access this port.
PXI/CLK10	 10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an FPGA I/O Node configured for reading to access this channel. Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start»All Programs»National Instruments»NI-RIO.
PXI/LBR <i>x</i>	Local bus right channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to

	access this channel.
PXI/LBLSTAR <i>x</i>	Local bus left channel <i>x</i> , where <i>x</i> is the channel number. If you are using the device in slot two of the PXI chassis, this channel is a star trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data</u> <u>Enable</u> method to access this channel.
PXI/STAR	Star trigger bus. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to access this channel.
	Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction.
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data Enable</u> method to access this channel. Follow the guidelines for <u>using PXI triggers with</u> the LabVIEW FPGA Module.

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u>.

NI PXI-7830R Reference

R Series Reconfigurable I/O Module (AI, AO, DIO)

4 AI channels, 4 AO channels, 56 DIO lines, 1 million gate FPGA, 200 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.
Connectorx/DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.
Connectorx/DIOPORTy	Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> channels. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set Data</u> Output or <u>Set Data Enable</u> method to access this port.
PXI/CLK10	10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an <u>FPGA I/O Node</u> configured for reading to access this channel.
	Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start »All

	Programs»National Instruments»NI- RIO.
PXI/LBR <i>x</i>	Local bus right channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set</u> Data Output or <u>Set Data Enable</u> method to access this channel.
PXI/LBLSTAR <i>x</i>	Local bus left channel <i>x</i> , where <i>x</i> is the channel number. If you are using the device in slot two of the PXI chassis, this channel is a star trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data</u> <u>Enable</u> method to access this channel.
PXI/STAR	 Star trigger bus. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel. Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction.
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data Enable</u> method to access this channel. Follow the guidelines for <u>using PXI triggers with</u> <u>the LabVIEW FPGA Module</u> .

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/O only.
NI PXI-7831R Reference

R Series Reconfigurable I/O Module (AI, AO, DIO)

8 AI channels, 8 AO channels, 96 DIO lines, 1 million gate FPGA, 200 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description	
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.	
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.	
Connectorx/DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.	
Connectorx/DIOPORTy	^r Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> <u>channels</u> . Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data</u> <u>Output</u> or <u>Set Data Enable</u> method to access this port.	
PXI/CLK10	10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an <u>FPGA I/O Node</u> configured for reading to access this channel.	
	Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start »All	

	Programs»National Instruments»NI- RIO.	
PXI/LBR <i>x</i>	Local bus right channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.	
PXI/LBLSTAR <i>x</i>	Local bus left channel <i>x</i> , where <i>x</i> is the channel number. If you are using the device in slot two of the PXI chassis, this channel is a star trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data</u> <u>Enable</u> method to access this channel.	
PXI/STAR	 Star trigger bus. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel. Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction. 	
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data Enable</u> method to access this channel. Follow the guidelines for <u>using PXI triggers with</u> <u>the LabVIEW FPGA Module</u> .	

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/O only.

NI 7831R Digital Port Assignments

You can use an FPGA I/O Node, configured for reading and writing, with the NI 7831R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39
Connector 2	DIOPORT 0	0 (LSB) through 7
Connector 2	DIOPORT 1	8 (LSB) through 15
Connector 2	DIOPORT 2	16 (LSB) through 23
Connector 2	DIOPORT 3	24 (LSB) through 31
Connector 2	DIOPORT 4	32 (LSB) through 39

NI PXI-7833R Reference

R Series Reconfigurable I/O Module (AI, AO, DIO)

8 AI channels, 8 AO channels, 96 DIO lines, 3 million gate FPGA, 200 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description	
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.	
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.	
Connectorx/DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.	
Connectorx/DIOPORTy	^r Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> <u>channels</u> . Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data</u> <u>Output</u> or <u>Set Data Enable</u> method to access this port.	
PXI/CLK10	10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an <u>FPGA I/O Node</u> configured for reading to access this channel.	
	Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start »All	

	Programs»National Instruments»NI- RIO.	
PXI/LBR <i>x</i>	Local bus right channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.	
PXI/LBLSTAR <i>x</i>	Local bus left channel <i>x</i> , where <i>x</i> is the channel number. If you are using the device in slot two of the PXI chassis, this channel is a star trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data</u> <u>Enable</u> method to access this channel.	
PXI/STAR	 Star trigger bus. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel. Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction. 	
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data Enable</u> method to access this channel. Follow the guidelines for <u>using PXI triggers with</u> <u>the LabVIEW FPGA Module</u> .	

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/O only.

NI 7833R Digital Port Assignments

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with the NI 7833R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39
Connector 2	DIOPORT 0	0 (LSB) through 7
Connector 2	DIOPORT 1	8 (LSB) through 15
Connector 2	DIOPORT 2	16 (LSB) through 23
Connector 2	DIOPORT 3	24 (LSB) through 31
Connector 2	DIOPORT 4	32 (LSB) through 39

NI PXI-7841R Reference

R Series Reconfigurable I/O Module (AI, AO, DIO)

8 AI channels, 8 AO channels, 96 DIO lines, LX30, 200 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description	
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.	
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.	
Connectorx/DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.	
Connectorx/DIOPORTy	^r Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> <u>channels</u> . Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data</u> <u>Output</u> or <u>Set Data Enable</u> method to access this port.	
PXI/CLK10	10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an <u>FPGA I/O Node</u> configured for reading to access this channel.	
	Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start »All	

	Programs»National Instruments»NI- RIO.	
PXI/STAR	Star trigger bus. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to access this channel.	
	Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction.	
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel. Follow the guidelines for using PXI triggers with the LabVIEW FPGA Module.	

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/O only.

NI 7841R Digital Port Assignments

You can use an FPGA I/O Node, configured for reading and writing, with the NI 7841R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39
Connector 2	DIOPORT 0	0 (LSB) through 7
Connector 2	DIOPORT 1	8 (LSB) through 15
Connector 2	DIOPORT 2	16 (LSB) through 23
Connector 2	DIOPORT 3	24 (LSB) through 31
Connector 2	DIOPORT 4	32 (LSB) through 39

NI PXI-7842R Reference

R Series Reconfigurable I/O Module (AI, AO, DIO)

8 AI channels, 8 AO channels, 96 DIO lines, LX50, 200 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.
Connectorx/DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.
Connectorx/DIOPORTy	Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> channels. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set Data</u> Output or <u>Set Data Enable</u> method to access this port.
PXI/CLK10	10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an <u>FPGA I/O Node</u> configured for reading to access this channel.
	Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start »All

	Programs»National Instruments»NI- RIO.	
PXI/STAR	Star trigger bus. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to access this channel.	
	Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction.	
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the <u>Set Data Output</u> or <u>Set Data Enable</u> method to access this channel. Follow the guidelines for <u>using PXI triggers with</u> the LabVIEW FPGA Module.	

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
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Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/O only.

NI 7842R Digital Port Assignments

You can use an FPGA I/O Node, configured for reading and writing, with the NI 7842R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39
Connector 2	DIOPORT 0	0 (LSB) through 7
Connector 2	DIOPORT 1	8 (LSB) through 15
Connector 2	DIOPORT 2	16 (LSB) through 23
Connector 2	DIOPORT 3	24 (LSB) through 31
Connector 2	DIOPORT 4	32 (LSB) through 39

NI PXI-7851R Reference

R Series Reconfigurable I/O Module (AI, AO, DIO)

8 AI channels, 8 AO channels, 96 DIO lines, LX30, 750 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description	
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.	
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.	
Connectorx/DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.	
Connectorx/DIOPORTy	 Digital input/output port y on connector x, where y is the port number and x is the connector number. A port is made up of <u>eight digital</u> <u>channels</u>. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data</u> <u>Output</u> or <u>Set Data Enable</u> method to access this port. 	
PXI/CLK10	10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an <u>FPGA I/O Node</u> configured for reading to access this channel.	
	Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start »All	

	Programs»National Instruments»NI- RIO.	
PXI/STAR	Star trigger bus. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to access this channel.	
	Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction.	
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel. Follow the guidelines for using PXI triggers with the LabVIEW FPGA Module.	

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

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Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/O only.

NI 7851R Digital Port Assignments

You can use an FPGA I/O Node, configured for reading and writing, with the NI 7851R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39
Connector 2	DIOPORT 0	0 (LSB) through 7
Connector 2	DIOPORT 1	8 (LSB) through 15
Connector 2	DIOPORT 2	16 (LSB) through 23
Connector 2	DIOPORT 3	24 (LSB) through 31
Connector 2	DIOPORT 4	32 (LSB) through 39

NI PXI-7852R Reference

R Series Reconfigurable I/O Module (AI, AO, DIO)

8 AI channels, 8 AO channels, 96 DIO lines, LX50, 750 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description	
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.	
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.	
Connectorx/DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.	
Connectorx/DIOPORTy	 Digital input/output port y on connector x, where y is the port number and x is the connector number. A port is made up of <u>eight digital</u> <u>channels</u>. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data</u> <u>Output</u> or <u>Set Data Enable</u> method to access this port. 	
PXI/CLK10	10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an <u>FPGA I/O Node</u> configured for reading to access this channel.	
	Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start »All	

	Programs»National Instruments»NI- RIO.	
PXI/STAR	Star trigger bus. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to access this channel.	
	Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction.	
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel. Follow the guidelines for using PXI triggers with the LabVIEW FPGA Module.	

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

 $\overline{\mathbb{N}}$

Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/ only.

NI 7852R Digital Port Assignments

You can use an FPGA I/O Node, configured for reading and writing, with the NI 7852R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39
Connector 2	DIOPORT 0	0 (LSB) through 7
Connector 2	DIOPORT 1	8 (LSB) through 15
Connector 2	DIOPORT 2	16 (LSB) through 23
Connector 2	DIOPORT 3	24 (LSB) through 31
Connector 2	DIOPORT 4	32 (LSB) through 39

NI PXI-7853R Reference

R Series Reconfigurable I/O Module (AI, AO, DIO)

8 AI channels, 8 AO channels, 96 DIO lines, LX85, 750 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Terminals in Software

You can select the following terminals for this device.

Terminal	Description	
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.	
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.	
Connectorx/DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.	
Connectorx/DIOPORTy	^r Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> <u>channels</u> . Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data</u> <u>Output</u> or <u>Set Data Enable</u> method to access this port.	
PXI/CLK10	10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an <u>FPGA I/O Node</u> configured for reading to access this channel.	
	Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start »All	

	Programs»National Instruments»NI- RIO.	
PXI/STAR	Star trigger bus. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to access this channel.	
	Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction.	
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel. Follow the guidelines for using PXI triggers with the LabVIEW FPGA Module.	

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

 $\overline{\mathbb{N}}$

Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description		
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.		
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.		
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.		
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.		
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.		

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/ only.

NI 7853R Digital Port Assignments

You can use an FPGA I/O Node, configured for reading and writing, with the NI 7853R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39
Connector 2	DIOPORT 0	0 (LSB) through 7
Connector 2	DIOPORT 1	8 (LSB) through 15
Connector 2	DIOPORT 2	16 (LSB) through 23
Connector 2	DIOPORT 3	24 (LSB) through 31
Connector 2	DIOPORT 4	32 (LSB) through 39

NI PXI-7854R Reference

R Series Reconfigurable I/O Module (AI, AO, DIO)

8 AI channels, 8 AO channels, 96 DIO lines, LX110, 750 kS/s AI Sample Rate

FPGA I/O Node

You can use an <u>FPGA I/O Node</u>, configured for reading and writing, with this device.



Note FPGA I/O Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.
Terminals in Software

You can select the following terminals for this device.

Terminal	Description	
Alx	Analog input channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading to access this channel.	
AOx	Analog output channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for writing to access this channel.	
Connectorx/DIOy	Digital input/output channel <i>y</i> on connector <i>x</i> , where <i>y</i> is the channel number and <i>x</i> is the connector number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel.	
Connectorx/DIOPORTy	^r Digital input/output port <i>y</i> on connector <i>x</i> , where <i>y</i> is the port number and <i>x</i> is the connector number. A port is made up of <u>eight digital</u> <u>channels</u> . Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set Data</u> <u>Output</u> or <u>Set Data Enable</u> method to access this port.	
PXI/CLK10	10 MHz clock in the PXI chassis that you can use to synchronize multiple PXI modules. Use an <u>FPGA I/O Node</u> configured for reading to access this channel.	
	Note You can phase lock the FPGA device clock to the 10 MHz clock of the PXI chassis. The FPGA clock synchronizes to the 10 MHz clock but does not change to 10 MHz. Refer to the <i>RIO Device Setup Help</i> for more information about synchronizing the FPGA clock to the 10 MHz clock. This help file is available from Start »All	

	Programs»National Instruments»NI- RIO.	
PXI/STAR	Star trigger bus. Use an <u>FPGA I/O Node</u> configured for reading or writing, or use the <u>Set</u> <u>Data Output</u> or <u>Set Data Enable</u> method to access this channel.	
	Caution Do not use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable to access the PXI/STAR channel if the FPGA device is in slot two of the PXI chassis. Writing to the PXI/STAR channel when the FPGA device is in slot two affects the accuracy of the 10 MHz clock and can cause the PXI system to malfunction.	
PXI/TRIG <i>x</i>	Trigger channel <i>x</i> , where <i>x</i> is the channel number. Use an FPGA I/O Node configured for reading or writing, or use the Set Data Output or Set Data Enable method to access this channel. Follow the guidelines for using PXI triggers with the LabVIEW FPGA Module.	

Arbitration

This device supports arbitration. Configure the arbitration settings for the channels of this device in the FPGA I/O Properties dialog box for the FPGA I/O item you are using.

I/O Methods

Use the <u>FPGA I/O Method Node</u> to invoke methods. You can use the following methods with this device.

 $\overline{\mathbb{N}}$

Note FPGA I/O Method Nodes cannot be configured to write to R Series digital output channels as both ports and lines. You must write digital outputs as either a port or a line.

Method	Description		
Set Output Data	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.		
Set Output Enable	Refer to the FPGA I/O Method Node (FPGA Module) topic for a description of this method.		
Wait on Any Edge	Pauses the execution of the I/O Method Node until the next falling or rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Any Edge method waits for the next falling or rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.		
Wait on Falling Edge	Pauses the execution of the I/O Method Node until the next falling edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Falling Edge method waits for the next falling edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.		
Wait on High Level	Pauses the execution of the I/O Method Node until the digital signal is high. The Timeout input specifies in FPGA clock ticks how long the Wait on High Level method waits for the next high level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.		

Wait on Low Level	Pauses the execution of the I/O Method Node until the digital signal is low. The Timeout input specifies in FPGA clock ticks how long the Wait on Low Level method waits for the next low level. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.
Wait on Rising Edge	Pauses the execution of the I/O Method Node until the next rising edge of the digital signal. The Timeout input specifies in FPGA clock ticks how long the Wait on Rising Edge method waits for the next rising edge. A value of 0 causes the method to timeout immediately, a negative value causes the method to wait indefinitely, and a positive value causes the method to wait for that number of clock ticks before timing out.

I/O Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the <u>Single-Cycle Timed Loop</u> for digital I/ only.

NI 7854R Digital Port Assignments

You can use an FPGA I/O Node, configured for reading and writing, with the NI 7854R. Use the following digital port assignments when you configure digital port functions.



Note Refer to the <u>NI R Series Intelligent DAQ User Manual</u> for information about connector pin assignments.

Connector	Digital Port	Digital Lines
Connector 0	DIOPORT 0	0 (LSB) through 7
Connector 0	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 0	0 (LSB) through 7
Connector 1	DIOPORT 1	8 (LSB) through 15
Connector 1	DIOPORT 2	16 (LSB) through 23
Connector 1	DIOPORT 3	24 (LSB) through 31
Connector 1	DIOPORT 4	32 (LSB) through 39
Connector 2	DIOPORT 0	0 (LSB) through 7
Connector 2	DIOPORT 1	8 (LSB) through 15
Connector 2	DIOPORT 2	16 (LSB) through 23
Connector 2	DIOPORT 3	24 (LSB) through 31
Connector 2	DIOPORT 4	32 (LSB) through 39

Using PXI Triggers with the LabVIEW FPGA Module

You can use the FPGA I/O Node to access the trigger lines on PXI R Series devices. When developing an FPGA VI that uses triggers, be sure to reserve the trigger lines you are using and, to ensure compatibility with other R Series devices, configure trigger pulses on PXI R Series devices to last for at least two clock cycles of the clock on the receiving device. Refer to the PXI Specification for more information about trigger bus requirements.

Configuring Trigger Pulses

To ensure compatibility with other NI R Series devices, configure trigger pulses on an NI PXI R Series device to last for at least two clock cycles of the clock on the receiving device. For example, if the clock on the receiving device is 80 MHz, which is a clock period of 12.5 nanoseconds, the trigger line must be constant for at least 25 nanoseconds, which is two cycles of an 80 MHz clock.

Note Regardless of the clock speed, pulses on the trigger line must be constant for at least 18 nanoseconds. Refer to the <u>PXI</u> <u>Specification</u> for more information about trigger timing parameters.

The clocks between a PXI R Series device and another PXI device might not be perfectly synchronized. If you assert a trigger line on a PXI R Series device, you cannot determine at what point in the clock period the trigger registers in the receiving flip-flop. If the trigger arrives during the setup or hold time of the receiving flip-flop, you cannot determine the state of the line for that clock period. Asserting the trigger pulse for two clock cycles ensures that at least one clock cycle on the receiving flip-flop registers as a rising edge and transfers as a trigger.

Reserving Trigger Lines for PXI R Series Devices

National Instruments recommends that you reserve the trigger lines used by NI PXI R Series devices. If two PXI devices try to drive the same trigger line in different applications, or if the PXI devices are not programmed to work together, the application will not work and, in some cases, third-party PXI devices can be damaged. You can use Measurement & Automation Explorer (MAX) or the host VI to reserve trigger lines.

Reserving Trigger Lines in MAX

If you download and run the FPGA VI interactively, configure the PXI triggers in MAX. MAX maintains the trigger reservation for the R Series device even after you cycle power to the PXI chassis.

Reserving Trigger Lines in the LabVIEW FPGA Host VI

If you download and run the FPGA VI programmatically, reserve the trigger lines in the host VI. Use the Invoke Method function to reserve the trigger and to release the trigger reservation. LabVIEW releases the trigger reservation for the R Series device automatically when you close the FPGA VI reference. You must run the host VI again to reserve the trigger.

Reserving Trigger Lines

Complete the following steps to reserve a trigger line for a PXI R Series device.

- 1. Place the <u>Open FPGA VI Reference</u> function on the block diagram and configure it for the FPGA device and FPGA VI.
- 2. Place the <u>Invoke Method</u> function on the block diagram.
- 3. Wire the **FPGA VI Reference Out** output of the Open FPGA VI Reference function to the **FPGA VI Reference In** input of the Invoke Method function.
- 4. Wire the **error out** output of the FPGA VI Reference function to the **error in** input of the Invoke Method function.
- 5. Click the Invoke Method function and select **Reserve PXI Trigger** from the shortcut menu.
- 6. Right-click the **Trigger** input and select **Create»Constant**. An <u>enum constant</u> is created to help you select the trigger.

To reserve multiple trigger lines, repeat steps 2 to 6 for each trigger line you want to reserve, wiring the **FPGA VI Reference Out** output of the existing Invoke Method function to the **FPGA VI Reference In** input of the Invoke Method node that follows it.

Releasing Trigger Lines

Complete the following steps to release a trigger line for a PXI R Series device.

- 1. Place the <u>Open FPGA VI Reference</u> function on the block diagram and configure it for the FPGA device and FPGA VI.
- 2. Place the Invoke Method function on the block diagram.
- 3. Wire the **FPGA VI Reference Out** output of the Open FPGA VI Reference function to the **FPGA VI Reference In** input of the

Invoke Method function.

- 4. Wire the **error out** output of the FPGA VI Reference function to the **error in** input of the Invoke Method function.
- 5. Click the Invoke Method function and select **Unreserve PXI Trigger** from the shortcut menu.
- 6. Right-click the **Trigger** input and select **Create»Constant**. An <u>enum constant</u> is created to help you select the trigger.

To release multiple trigger lines, repeat steps 2 to 6 for each trigger line you want to release, wiring the **FPGA VI Reference Out** output of the existing Invoke Method function to the **FPGA VI Reference In** input of the Invoke Method node that follows it.

Calibrating NI 78xxR Devices

Refer to the <u>NI 78xxR Utilities Help</u> for information about calibrating your NI 783xR/784xR/785xR device.

This help file is also available at **Start»All Programs»National Instruments»NI-RIO**.

Using Set Output Data and Set Output Enable

All of the digital lines on the R Series devices are bi-directional. These lines can be individually configured for input or output. Internal to the R Series device, a Digital Enable (DE) signal controls whether the line is configured for input or output. When the DE is set to True, the digital line is configured as an output, and the value stored in Digital Data (DD) will be driven on the digital line. When the DE is set to False, the digital line is configured as a high-impedance input allowing the line to be driven by an external device. Regardless of the state of the DE, the Digital Input (DI) can be monitored to observe the current state of the digital line.

The following figure shows how the Digital Input (DI), Digital Data (DD), and Digital Enable (DE) signals operate to control a single digital line on the I/O connector.

DI _____ Connector DE _____

When an FPGA I/O Node configured for output is executed, the data written to the FPGA I/O Node is written to the DD of the digital line, and the DE for the digital line is automatically set to True. This causes the line to be configured as an output driving the specified data. When an FPGA I/O Node configured for input is executed, the current state of the digital line is sampled using the DI signal and returned by the FPGA I/O Node. The DE value is not updated by an FPGA I/O Node configured for input.

If you need more precise control over the DD and DE signals, use the <u>Set</u> <u>Output Data</u> and <u>Set Output Enable</u> methods. The Set Output Enable method takes the value wired to the input of the method and writes it to the DE control signal. This allows you to change the direction of the digital line without affecting the data on the line. The Set Output Data method takes the value wired to the input of the method and writes it to the DD signal. This allows you to change the data driven on the line when the line is configured as an output without affecting the currently configured direction (DE).

Two-Way Communication

To perform two-way communication, after executing an FPGA I/O Node configured for output, run a Set Output Enable method with a False wired to the input before allowing the line to be powered externally. After this step, you can read the input value using an FPGA I/O Node configured for input. When the line is no longer powered externally, you can configure the line for output again using either an FPGA I/O Node configured for output or by running a Set Output Enable method with a True wired to the input.