# **NI-IMAQ I/O Terminal Reference**

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This book contains information about using an NI-IMAQ I/O device with LabVIEW and the LabVIEW FPGA Module.

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# **NI-IMAQ I/O Reference**

The following information pertains to the reconfigurable I/O module on your NI-IMAQ I/O device.

## **FPGA Targets**

NI-IMAQ I/O devices use one of two FPGA targets, depending on which device you have. The following table describes which target to use for your NI-IMAQ I/O device.

FPGA Target	NI-IMAQ I/O Devices
IMAQIO–5	NI 1454
	NI 1455 Revision D and higher
	NI 1456 Revision D and higher
	NI 8254R
	NI 8255R
IMAQIO-1	NI 1455 Revision A, B, or C NI 1455 Revision A, B, or C

## FPGA I/O Node

The <u>FPGA I/O Node</u> is used to control the digital inputs and digital outputs provided by the NI-IMAQ I/O device.



**Note** In LabVIEW 8.*x*, the FPGA I/O Node automatically enables TTL Output lines. For low-level control of the TTL Output Enables, use <u>FPGA I/O Methods</u>.



**Note** In LabVIEW 7.*x*, use the Digital Input and Digital Output FPGA device I/O functions to control all digital I/O.

# **Terminals in Software**

You can select the following terminals for the NI-IMAQ I/O device:

Terminal	Description
TTL_IN_x	TTL-level digital input line <i>x</i> . There are two TTL input lines available through the 44-pin D-Sub connector. Refer to your NI-IMAQ I/O hardware documentation for the 44-pin D-Sub connector pinout.
TTL_OUT_X	TTL-level digital output line <i>x</i> . There are 10 TTL output lines, with <07> available on the 44-pin D-Sub connector, and TTL_OUT_9 connecting to TRIG 1 and TTL_OUT_8 connecting to TRIG 2. Refer to your NI-IMAQ I/O hardware documentation for the 44-pin D- Sub connector pinout.
ISO_IN_X	Isolated digital input line <i>x</i> . There are 13 isolated input lines, with <011> available on the 44-pin D-Sub connector, and ISO_IN_12 connecting to TRIG 0. Refer to your NI-IMAQ I/O hardware documentation for the 44-pin D- Sub connector pinout.
ISO_OUT_x	Isolated digital output <i>x</i> . There are four isolated output lines available through the 44- pin D-Sub connector. Refer to your NI-IMAQ I/O hardware documentation for the 44-pin D- Sub connector pinout.
USER_DIP	Boot-up value of the User 1 DIP switch on the front panel of the NI-IMAQ I/O device. This value is only updated when the system boots. Switching the DIP switch while running is not reflected in the FPGA. This terminal is valid only valid on NI CVS-
ISO DOWED DDESENT	1450 Series compact vision systems.
ISO_POWER_PRESENT	value is <b>IRUE</b> when isolated power is

	provided to the power connector. Value is <b>FALSE</b> when isolated power is not provided.
SYSTEM_SHUTDOWN	Puts the system in a shutdown state. This is useful for implementing custom watchdog applications. This terminal is valid only when shutdown is
	enabled.

## Arbitration

NI-IMAQ I/O devices support arbitration on the output lines. Since all inputs are unidirectional, the default value is **Always Readable**. Configure the arbitration settings for the NI-IMAQ I/O device channels in the **Configure** dialog box for the FPGA device I/O function you are using.

## **FPGA I/O Methods**

FPGA I/O Methods are used for low-level control of the TTL Output lines. Use the FPGA I/O Method Node to control the TTL Output Enables and TTL Output Data.



**Note** FPGA I/O Methods are not supported by NI-IMAQ I/O devices in LabVIEW 7.*x*. Use the Digital Output FPGA device I/O function to enable and disable TTL Output lines.

# **I/O Properties**

NI-IMAQ I/O devices do not support any I/O properties.

## **Memory and Interrupts**

NI-IMAQ I/O devices support access to on-chip memory through the <u>Memory Read</u> and <u>Memory Write</u> VIs, and interrupts using the <u>Interrupt</u>  $\underline{VI}$ .



**Note** The Interrupt VI is not supported in LabVIEW 7.*x*.

### **DMA FIFOs**

NI-IMAQ I/O devices support direct memory access (DMA) FIFOs to transfer data to and from the FPGA VI to the host VI. There are three DMA channels available to NI-IMAQ I/O devices.



**Note** DMA FIFOs are supported in LabVIEW 8.0 and later with NI-IMAQ I/O 2.0 and later.

# Single-Cycle Timed Loop

NI-IMAQ I/O devices support the Single-Cycle Timed Loop.