



FPGA Timekeeper API

June 2012, 373814A-01

The FPGA Timekeeper API is a set of VIs that allow you to synchronize time on your FPGA targets. This release includes an LabVIEW project library (.lvlib) that contains these VIs, as well as an example project and VIs that allow you to control the time on your FPGA target through a LabVIEW Real-Time target.

Software Requirements

The FPGA Timekeeper API requires the following software components:

- LabVIEW 2010 or later
- LabVIEW 2010 FPGA Module or later

The LV FPGA Timekeeper examples also require the following additional software components:

- LabVIEW 2010 Real-Time Module or later
- NI-RIO 12.0

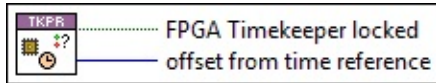
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Get Status (VI)

Installed With: FPGA Timekeeper

Provides the status of the current state of the FPGA Timekeeper.

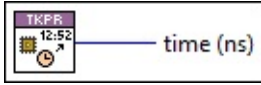



- offset from time reference** provides the measured offset in nanoseconds between the FPGA Timekeeper and the time reference. This measurement occurs each time the Sync Time VI is called.
- FPGA Timekeeper locked** is TRUE if the FPGA Timekeeper has locked on to and is tracking the given time reference.

Get Time (VI)

Installed With: FPGA Timekeeper

Returns the current time of the FPGA Timekeeper.

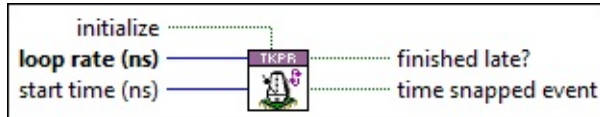


 **time (ns)** is the current time of the FPGA Timekeeper.

Metronome (VI)

Installed With: FPGA Timekeeper

Synchronizes execution rate of a loop.



TF **initialize** initializes the metronome to start from the given start time.

U32 **loop period (ns)** sets the loop control rate.

U64 **start time (ns)** sets the start time for the first iteration of the calling loop structure. If the start time is zero, the first iteration will begin on the next loop rate boundary. For example, with a start time of zero and a loop rate of one second (1,000,000,000 ns), the metronome will begin on the next second's boundary.

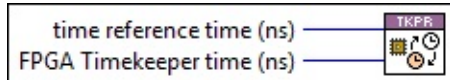
TF **finished late?** is TRUE if the previous loop iteration finished late.

TF **time snapped event** is TRUE if a discontinuity in time has occurred. Provide a new start time and set the **initialize** terminal to TRUE.

Sync Time (VI)

Installed With: FPGA Timekeeper

Synchronizes the FPGA Timekeeper to a Time Reference (i.e. GPS, RT, ...). To synchRONize the FPGA Timekeeper to a Time Reference, call this VI periodically with the time of the Time Reference and the correlating time of the FPGA Timekeeper.



U64 **time reference time (ns)** specifies the time of the time reference. The FPGA Timekeeper is synchronized to the time reference.

U64 **FPGA Timekeeper time (ns)** specifies the time of the FPGA Timekeeper.

Timekeeper (VI)

Installed With: FPGA Timekeeper

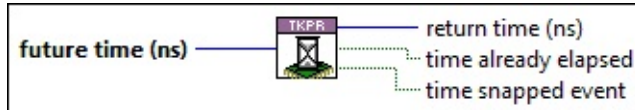
The FPGA Timekeeper allows you to synchronize time on your FPGA targets. Place this VI in the top-level VI outside of all block diagram structures.



Wait for Time (VI)

Installed With: FPGA Timekeeper

Waits for the given time to arrive.



- U64** **future time (ns)** specifies the time to wait in nanoseconds.
- TF** **time already Elapsed** is TRUE if this VI is called with a time that is in the past.
- U64** **return time (ns)** is the time of the FPGA Timekeeper when this VI completed.
- TF** **time snapped event** is TRUE if a discontinuity in time has occurred.